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Abstract

Japan, once the global leader in semiconductors, has re-emerged as a major player in industrial policy for chips amid supply chain shocks and rising geopolitical competition. This paper examines the historical trajectory of Japan's semiconductor industry, its decline from dominance in the 1980s and its current revival strategies. We analyze the drivers of past success and the subsequent erosion of competitiveness due to trade disputes, structural rigidities and missed transitions to new business models. Against this backdrop, the paper describes Japan's recent interventions, including subsidies, tax incentives and public–private partnerships, with a particular focus on the Japan Advanced Semiconductor Manufacturing fabrication plants in Kumamoto and the Rapidus project in Hokkaido. These initiatives highlight contrasting models of international collaboration and domestic technological ambition, raising questions about risk, sustainability and integration with global value chains. We assess progress to date, challenges in financing, human capital, technological feasibility and the implications of Japan's strategy for global semiconductor governance. The paper concludes by distilling lessons for effective industry policy, emphasizing openness, diversification, performance-linked support and the importance of international cooperation in avoiding subsidy races while building resilient ecosystems.

Keywords: semiconductors, Rapidus, industrial policy

JEL classification: O3, O25, L52

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Introduction

The global semiconductor industry is shaped not only by rapid technological advances but also intensifying geopolitical competition and the experience of disruptions to supply chains. Japan, once the undisputed leader in semiconductor manufacturing, has embarked on an ambitious policy push to revive its position in this industry. This paper examines the evolution of Japan's semiconductor industry, the motivations and mechanisms behind recent government interventions and the outcomes and lessons that can inform the design of effective industry policy.

Japan dominated the semiconductor domain in the 1970s and 1980s. Innovation, investment and, to a lesser extent some collaborative research and development (R&D) among major firms positioned Japan at the forefront of memory chip production (Tomoshige, 2022; Chang, 2025). However, a combination of external pressures – such as the US–Japan Semiconductor Trade Agreement in 1986, currency appreciation and the rise of global competitors – and internal challenges, including over-standardisation and slow adaptation to new business models, led to a dramatic erosion of Japan's market share by the 2000s (Koh, 2024, p.76). Today, Japan's chip production is concentrated in mature nodes (12–40nm), while the technological frontier – defined by 3nm and approaching 2nm chips for AI and high-performance computing – is dominated by firms in Taiwan, South Korea and the United States (Grant-Chapman and McGee, 2024; Satoh and Ting-Fang, 2024).

The resurgence of industrial policy in Japan's semiconductor sector is driven by several factors. The COVID-19 pandemic exposed vulnerabilities in global supply chains, particularly for automotive and industrial chips. Meanwhile, escalating geopolitical tensions have increased attention to the national security interests in domestic semiconductor production and ensuring access to semiconductors (Huang, 2024). In response, Japan has launched a series of large-scale interventions, including direct subsidies, tax incentives, R&D funding and public–private partnerships to attract advanced manufacturing capabilities and rebuild a competitive ecosystem. Notable projects include the TSMC/Sony/Denso JASM fabrication plants (fabs) in Kumamoto, which leverage international collaboration to rapidly scale up production, and the Rapidus initiative in Hokkaido, a bid to leapfrog to 2nm logic chip manufacturing with support from global technology leaders (METI, 2024, pp.6-7; Chang, 2025).

The purpose of this paper is threefold. First, we analyse the historical trajectory and current state of Japan's semiconductor industry, considering the interaction between government policy, industry structure and technological innovation. Second, we evaluate the design, implementation and early outcomes of Japan's recent semiconductor policy interventions, including both foreign-led (JASM) and domestic-led (Rapidus) projects to identify challenges that may impact the prospects for success. And finally, we distil key lessons for industry policy, drawing on Japan's experience and situating it within the broader context of global industrial policy competition.

The following sections review the evolution of the chip sector in Japan, the motivations for and the forms of the recent intervention, the progress to date and aspects of risks now faced. The regional context of this intervention is also stressed. Then follows a conclusion with outlines the lessons learned.

Evolution of Semiconductor Chips

The earliest phase of chip design and production began with discrete transistors – tiny electronic switches that replaced vacuum tubes in the 1950s. In the late 1950s, the invention of the integrated circuit (IC) – a single chip containing many transistors and other components – enabled the creation of more complex, reliable and compact electronic devices (Atherton, 1984, p.237). In the 1970s and 1980s, the industry advanced to the mass production of memory chips such as dynamic random-access memory (DRAM) for storing larger amounts of data and static random-access memory (SRAM) for smaller collections of data but offering high-speed access. Demand for these chips was supported by the rapidly growing computer and consumer electronics markets (Semiconductor History Museum of Japan, no date-a).

As the industry matured, reducing the process node – the smallest feature size on a chip, measured in nanometers (nm) – became a key benchmark of technological progress. Each reduction in node size allowed more transistors to be packed onto a chip, increasing performance and reducing power consumption (Han et al., 2024, p.1431). The current technological frontier is defined by chips produced at 3nm and 2nm nodes, manufactured using extreme ultraviolet (EUV) lithography – a process that uses very short-wavelength light to etch extremely fine patterns on silicon wafers. These chips are essential for high-performance computing, artificial intelligence (AI) and advanced consumer electronics. Only a few companies – TSMC, Samsung and Intel – have technologies to produce chips at these advanced nodes at commercial scale (Solís and Duchâtel, 2024).

Chip design and the impact of AI

The rapid growth of AI is now the dominant force shaping the evolution of semiconductor technology. AI workloads, such as training large machine learning models and processing massive amounts of real-time data, demand unprecedented levels of computational power, speed and energy efficiency (Grant-Chapman and McGee, 2024). Traditional CPUs, while powerful, are not optimised for the highly parallel and data-intensive nature of AI tasks. This has driven the development of specialised processors, including Graphics Processing Units (GPUs), Tensor Processing Units (TPUs) and AI Accelerators and Neural Processing Units (NPUs), which are designed for real-time AI processing in edge devices (Grant-Chapman and McGee, 2024; METI, 2024, pp.18-19).

These AI-focused chips leverage the most advanced semiconductor technologies, including 3nm and 2nm nodes, GAA transistors and advanced packaging techniques like chiplets and 3D stacking (METI, 2024, p.15; Solís and Duchâtel, 2024). AI's requirements are so intensive that they are accelerating the pace of semiconductor innovation beyond what traditional scaling (Moore's Law – the doubling of transistors every two years) could

achieve. Chipmakers are now focusing on new architectures, parallel processing and tighter integration between hardware and software to deliver the necessary performance and efficiency (Talati, 2021, p.98).

Furthermore, AI is not just a consumer of advanced chips: it is also transforming the way chips are designed and manufactured. AI-driven design tools automate complex tasks, optimise layouts, and enhance defect detection, speeding up the development cycle and improving yield (Raghuwanshi, 2024). This feedback loop – where AI drives chip innovation and advanced chips enable more powerful AI – has become a defining feature of the modern semiconductor industry.

Japan's Position Relative to the Frontier Over Time

By 1960, Japanese companies like Toshiba and Mitsubishi Electric were already developing expertise, producing semiconductors with US licences and sending researchers to the United States to better understand the production process (Hoeren, 2016, p.157). Japan had become the largest producer of transistors – a key component of integrated circuits – and had taken 50 per cent of the US market for portable radios (Morris, 2008, p.100). While these companies had established R&D programs, their budgets remained low relative to US R&D expenses. Sensing that better access to US research would require an exchange, the late 1960s saw a semiconductor 'research wave' begin in Japan (Hoeren, 2016, pp.159-160).

The global semiconductor industry changed considerably throughout the 1970s and 1980s. At the turn of the 1970s, most semiconductor companies were integrated device manufacturers (IDMs) – firms that were vertically integrated across large parts of the supply chain (Boston Consulting Group and Semiconductor Industry Association, 2021, p.11). The late 1970s then saw the 'second-phase' of the industry's organisation, where semiconductor equipment makers 'emerged as a distinct sub-sector' (Arita and Fujita, 2001, p.89). During these two phases, the United States, Europe and Japan dominated the semiconductor industry, collectively accounting for over 90 per cent of global production (Hart, 1989, p.131).

Things changed again in the mid-1980s. Developments in design-stage technologies supported a wider offering of integrated circuit products, opening market niches for new businesses. The contemporaneous 'rapidly rising costs' for manufacturing equipment contributed to the emergence of the fabless-foundry model, where firms in East Asia were subcontracted by US firms to manufacture custom-designed integrated circuits (Arita and Fujita, 2001, pp.89, 91-92).

These were the golden years for Japanese semiconductor manufacturing. In 1980, Japan had roughly one quarter of the global semiconductor industry, while the United States held over half the market (Semiconductor History Museum of Japan, no date-a). The next year, Japan's semiconductor exports 'exceeded those of the United States for the first time' (WTO, 1988, p.4). And, by 1986, Japan had surpassed the United States to become the largest supplier in the global semiconductor industry, accounting for 48 per cent of the market (Hart, 1989, p.131).

Perhaps the most notable success in Japan's semiconductor industry during this period was in the DRAM market. DRAMs are a type of semiconductor memory that were crucial to the computer industry in the 1970s and 1980s. In 1978, Japan accounted for roughly 25 per cent of the global DRAM market (Bridwell and Richard, 1998, p.25). Over the following decade, US manufacturers shifted their investments away from DRAMs and towards 'high-end computer chips' while Japanese firms expanded their DRAM production for their own internal use in their electronic products (Bridwell and Richard, 1998, p.44). The increased demand for memory production and domestic demand for consumer electronics thus drove the rising DRAM demand in Japan. Between 1983–4, demand for Japan's semiconductor products increased by approximately 150 per cent and, by 1987, Japan had attained technological superiority in 'design and process' tools and accounted for roughly 80 per cent of the global DRAM market (Semiconductor History Museum of Japan, no date-a).

The global dominance of Japanese firms during the period when DRAM devices served as the technological and commercial backbone of the semiconductor industry was underpinned by superior process engineering capabilities, abundant access to long-term bank credit and strong domestic demand – particularly from Nippon Telegraph and Telephone's (NTT) telecommunications expansion – which together fostered a dense ecosystem of equipment and materials suppliers. This vertically integrated industrial base enabled Japan to consolidate its comparative advantage in memory production. As long as DRAMs remained the industry's central product, Japanese producers were effectively unrivalled – until the emergence of Korean entrants reshaped competitive dynamics.

The contribution of government industry policy, government-led R&D, collaborative projects like the VLSI initiative – see Box A – towards these developments in Japan are contested (Koh, 2024, p.76; Chang, 2025). The Japanese government's investment in R&D and the pooling of resources among major firms contributed to assessments that Japan Inc had a unique and unfair model to reach the forefront of the global industry and contributed to the US justification for protectionism against Japan in the 1986 U.S. Japan semiconductor trade agreement .

Box A: VLSI

The Very Large Scale Integration (VLSI) initiative was a Japanese government-led program launched in 1976 to accelerate the country's semiconductor industry through collaborative research and development. The Ministry of International Trade and Industry (MITI) sensed that Japan's computer and semiconductor manufacturers would struggle to compete internationally. It thus sought to 'expedite the development of core technologies and … realign the industry' (Gresser, 1980, p.16).

This initiative brought together Japan's leading semiconductor and computer companies – including Fujitsu, Hitachi, NEC, Mitsubishi Electric, NTT and Toshiba – to form the Super LSI Technology Research Association and jointly operate a laboratory in Kanagawa Prefecture (Tomoshige, 2022). The project aimed to develop

advanced technology for producing integrated circuits at large scale, which were crucial for the next generation of computers and electronics. Estimates of the public subsidies in the VLSI project vary, but are typically approximated at US$150 million between 1976–9 (Borrus, Millstein and Zvsman, 1983, p.181; Morris, 2008, p.104).

The VLSI program was notable for pooling R&D resources across major firms, fostering cooperation among traditional rivals and focusing on fundamental technology for semiconductors. Over four years, it received significant public and private funding and resulted in major technological breakthroughs, such as the development of electron beam lithography (EBL), which revolutionised chip-making equipment and paved the way for manufacturing 'more complex semiconductors at scale' (Tomoshige, 2022). The collaborative model of the VLSI initiative aimed to have Japanese firms develop a common technology platform and share information, to drive rapid innovation and contribute to Japan's dominance in the global semiconductor market by the late 1980s, when Japanese companies accounted for more than half of worldwide sales (Koh, 2024, p.76).

Koh (2024, p.76) highlights that the VLSI initiative was 'instrumental in pooling R&D across major semiconductor firms and produced technological breakthroughs', particularly in dynamic random-access memory (DRAM) technology. Japanese firms were the first to release 64K and 256K DRAMs into the market (Hart, 1993, p.80), and the program was viewed in the United States as a factor in Japan's rise to overtake US market share by the late 1980s. Nevertheless, companies did not send their best people to staff the various cross-company consortia or government collaboration efforts (Tomoshige, 2022; Suzuki, 2025). When Japanese firms could meet international competition without depending on government support, they were able to resist government efforts to influence their strategies, and the joint research endeavours halted (Hart, 1993, pp.83-84).

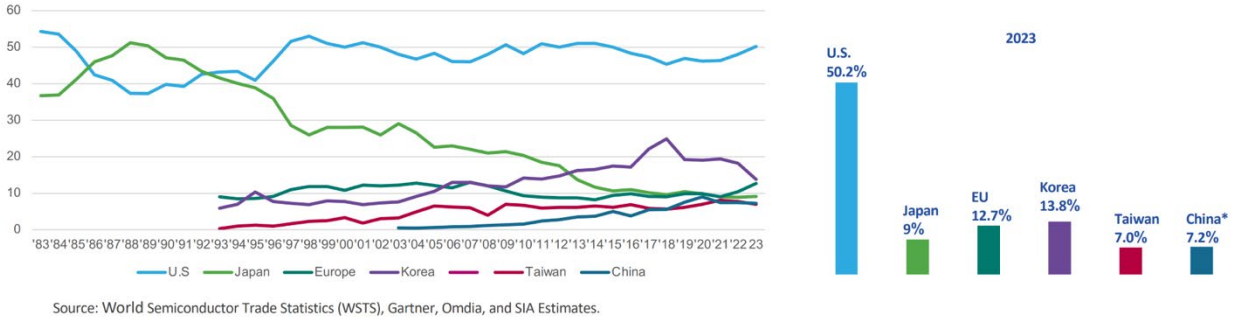
The notable exception where consortia succeeded was Sematech in the United States during a critical period in the 1990s. Sematech was established as a strategic initiative by the U.S. government to counter Japan's growing dominance in the semiconductor industry. Although it initially received federal funding, the consortium did not gain significant momentum until Robert Noyce—co-founder of Intel—resigned from Intel to lead the organization. Noyce leveraged his influence within the industry to restructure Sematech, discontinuing government funding and compelling major U.S. semiconductor firms to contribute financially and allocate top engineering talent. In a national context where industrial collaboration is often limited, Noyce's leadership was instrumental in revitalizing the domestic semiconductor sector. Sematech played a pivotal role during this era. By contrast, Japan's VLSI projects did not succeed in replicating this model.

In addition, Japanese policymakers both shielded the domestic market from foreign penetration while purchasing large amounts of foreign technology (Borrus, Millstein and Zvsmanm, 1983, p.200). MITI mandated that any licencing by foreign – generally US – firms had to be provided to all Japanese firms that requested its access, accelerating the 'diffusion of technology and knowledge' in the domestic market (Medina, 2011, p.44).

Finally, the keiretsu business structure (Hart, 1993, p.44) supported the Japanese overtaking of US semiconductor manufacturers in the 1980s. Japan's large electronics firms were connected to banks within their business groups that provided more favourable terms for accessing capital, allowing Japanese firms to 'pursue costly long-term strategies' (Brown and Linden, 2009, p.16; 2010, p.15). Further, the closer ties between semiconductor firms and their suppliers in the Japanese industry were viewed as supporting marginal improvements in the manufacturing process (Hart, 1993, p.130).

The position of Japan since the early 1980s is illustrated in Figure 1. Around 1988, Japanese firms such as NEC, Toshiba, and Hitachi controlled over 50 per cent of the global semiconductor industry, surpassing the United States (Access Partnership, 2022; Grant-Chapman and McGee, 2024).

Figure 1: Global Market Shares of the semiconductor industry, 1983 to 2023



Source: SIA-2024-Factbook.pdf

As DRAM markets matured, time-to-market for successive generations (64K, 256K, 1M, 4M) became the decisive variable in sustaining profitability. Each innovation cycle began with high margins that rapidly declined as prices converged toward marginal cost, producing a 'race to the bottom'. Survival increasingly depended on the capacity to undertake massive, recurring capital investments required to sustain technological upgrading in line with Moore's Law. US producers such as Mostek and National Semiconductor exited not because of deficiencies in design capability, but because they lacked the financial depth and industrial coordination mechanisms to sustain continuous investment. Japanese firms, supported by keiretsu financing structures, weathered these pressures through the 1990s. Meanwhile, the 1997 financial crisis triggered consolidation in Korea: Samsung emerged as the dominant player, while state-led restructuring merged weaker firms into what became SK Hynix.

The 1986 U.S.-Japan Semiconductor Agreement, prompted by US accusations of dumping on international markets and a protected market at home, imposed price controls (see Box B) and limited export volumes in the US market, forcing Japan to work to increase the US market share in the Japanese market (Tomoshige, 2022; Koh, 2024, p.76). These price controls and export restraints made Japanese DRAMs less competitive

internationally. As a result, South Korean companies – most notably Samsung and later SK Hynix – were able to enter the global market with lower-priced DRAM chips, rapidly gaining market share that had previously been dominated by Japanese firms (Park, 2019). The rapid appreciation of the yen after the 1985 Plaza Accord made Japanese exports more expensive, further undermining competitiveness by reducing the profits necessary for further investments in capital and innovation (Park, 2023, p.9).

Box B: Price Controls in the 1986 U.S.-Japan Semiconductor Agreement

The 1986 U.S.-Japan Semiconductor Agreement imposed price controls by requiring Japanese semiconductor manufacturers to sell certain types of chips, especially DRAMs, at or above a set minimum price – known as a 'floor price' – in the US market and in third-country markets. This was intended to stop what the United States alleged was 'dumping', or selling chips below cost, which harmed American producers (Johnson, 1994; Irwin, 1996, p.5; Tomoshige, 2022).

Under the agreement, the Japanese government committed to monitor and enforce these minimum prices for its companies' semiconductor exports. The US government, in turn, had the authority to set and oversee these minimum 'fair market value' prices. Japanese firms were prohibited from selling below these levels. If they did, they risked trade retaliation, such as the 100 per cent tariffs the United States imposed in 1987 when it judged Japan was not fully complying (Irwin, 1996, p.11; Koh, 2024, p.76; Tomoshige, 2022).

These price controls raised the cost of Japanese chips in the US and other markets, making them more expensive for American computer makers. At the same time, the agreement forced Japanese authorities to encourage domestic firms to buy more foreign-made chips, with the goal of increasing the foreign share of the Japanese semiconductor market from 10 to 20 per cent (Johnson, 1994; Irwin, 1996, p.5; Tomoshige, 2022; Koh, 2024, p.76).

From the late 1990s onward, the global semiconductor industry transitioned toward a disintegrated structure. The escalating fixed costs of fabrication, combined with shortening product cycles, induced a separation between design and manufacturing. Device firms increasingly outsourced production to specialised foundries, giving rise to the fabless–foundry model. Even integrated producers such as Advanced Micro Devices divested their fabrication facilities to focus on high-value activities such as chip architecture and marketing. This structural shift redefined comparative advantage in the industry – favouring firms with superior design and intellectual property capabilities – and paved the way for a new generation of U.S. technology leaders, including Qualcomm, Broadcom and Nvidia.

By 2023, Japan's share of global semiconductor sales had declined to less than 10 per cent, with no Japanese companies among the top ten by revenue (Koh, 2024, p.76). Japan's chip production in 2023 remained focused

on mature nodes (40nm). These are used in automotive, industrial and some consumer applications, but are not at the leading edge for AI, data centres or the most advanced consumer electronics (Koh, 2024, p.80; Chang, 2025). The most advanced chips for these applications – at 3nm and 2nm – are still produced by TSMC, Samsung and Intel outside Japan (Shivakumar, Wessner and Howell, 2023, p.2; Solís and Duchâtel, 2024).

The following section examines some of the other drivers of Japan's decline.

The Global Industry Shift and Japan's Decline

The global industry shifted from vertically integrated models to fabless–foundry specialisation, a transition led by Taiwan's TSMC. Japanese firms were slow to adapt, remaining focused on DRAM and missing the logic chip and foundry revolutions of the PC and smartphone eras that would have provided capital for further R&D (Tomoshige, 2022; Grant-Chapman and McGee, 2024).

Japanese companies, unlike those of other countries, failed to adapt to the vertical disintegration trend. This was not necessarily for lack of trying on the part of the Japanese government, which made several attempts during this period to encourage specialisation and reduce 'duplicative investment[s] in manufacturing infrastructure' (Tomoshige, 2022). Where mergers were attempted, the new companies often continued to act like separate entities or reportedly lacked strong leadership (Satoh and Ting-Fang, 2024). For the most part, though, semiconductor manufacturers 'clung to a broad portfolio of chips' rather than focusing their productive capabilities (Brown and Linden, 2010, p.19). Another ongoing feature of Japan's semiconductor industry was its grounding in the keiretsu structure – being dominated by large general electronics companies that did not specialise in producing semiconductors (Arita and Fujita, 2001, p.91). The keiretsu structure was favourable for promoting sales opportunities within business group networks but came to represent a weakness as Japan's economic growth slowed throughout the 1990s (Brown and Linden, 2010, p.19). Relatedly, cultural preferences that favoured a supply chain squarely within Japan are viewed as a factor that hampered Japan's ability to bring down its production costs for its high-quality DRAMs. In opting for automation of assembly, Japanese semiconductor companies were viewed as relatively slower than their US rivals in relocating operations to take advantage of lower-cost regions in Asia despite their superior geographical proximity (Brown and Linden, 2010, p.33).

Japanese firms engaged in contract semiconductor manufacturing for fabless companies but sought detailed knowledge of the products they fabricated, generating apprehension among fabless firms that Japanese producers might appropriate proprietary technologies for their own use (Brooks, 2000). As Van Agtmael (2007) observes, chip designers often feared that Japanese fabricators could misappropriate intellectual property, leading to persistent hesitation among semiconductor firms to outsource production to Japan.

In contrast, TSMC was institutionally constrained by its charter from designing or selling integrated circuits under its own name. This structural separation enabled TSMC to assure clients that it operated purely as a

manufacturing partner rather than a potential competitor (Van Agtmael, 2007). By design, this governance arrangement fostered trust with upstream design firms, distinguishing TSMC from its Japanese counterparts and underpinning its rise as a reliable global foundry.

Another crucial factor in the decline of Japan's semiconductor industry was the falling importance of DRAMs, which limited Japan's ability to exert some market power over semiconductor manufacturing technology (Chon, 1997, p.34). The emergence of 'alternative process drivers like static random access memory' and a narrowing 'process gap … between DRAMs and logic devices' caused this shift (Chon, 1997, p.33). In addition, Japanese companies competed in mainframe rather than personal computers (PCs), the latter being the major global growth market of the 1990s (Brown and Linden, 2010, p.19). Due to differences in memory chip configuration, Japan's DRAM requirements for its consumer electronics were incompatible with PC makers outside of Japan (Brown and Linden, 2010, p.19-20). Improvements in information storage capacities reduced the need for function-specific semiconductors. The industry shifted to system LSI (large-scale integrated circuit) chips, which contained various parts of an integrated circuit (Okada, 2008, p.39-40). As a result, other advanced countries could more easily manufacture semiconductors (Chon, 1997, p.34). Microprocessors and LSI chips became the source of competitiveness for the United States, which profited greatly from their increased demand (Lim, 2023, p.48). The move away from mainframes to PCs also disadvantaged Japan due to the shifting emphasis from quality and long-term reliability – where Japan was renowned – to low prices due to shorter product life spans (Cole and Matsumiya, 2007, p.80; Brown and Linden, 2010, p.19). Furthermore, Japan's focus on advancing process technologies hamstrung its ability to develop DRAMs at 'reduced prices and sizes, as Micron Technology and Korean companies had done' (Okada, 2008, p.72).

As Japan's semiconductor industry declined, its ability to finance R&D investments decreased (Kamakura, 2022, p.268). Matters were only exacerbated by the credit crunch induced by the asset bubble bursting in the early 1990s (Brown and Linden, 2010, p.18). Both factors made it more difficult for Japanese firms to raise funds for capital spending and accelerated R&D. South Korea and Taiwan dramatically increased capital equipment spending and captured Japan's ebbing market share (Kamakura, 2022, p.268). By 1998, South Korea had surpassed Japan in the global DRAM market (Semiconductor History Museum of Japan; no date-b). Much like Japan's semiconductor industry in the 1970s and 1980s, the entry and rise of the South Korean and Taiwanese industries were assisted by large-scale industrial policy and supportive domestic capital markets (Kamakura, 2022, p.265; Yeung, 2022, p.288).

The push for joint government-industry projects, while initially beneficial, eventually led to technological standardisation, reducing diversity and innovation within the sector. As the industry contracted, experienced engineers left for opportunities in Taiwan, South Korea, and China – a problem compounded by Japan's declining birthrate and aging population (Koh, 2024, p.80). Rising competition from new entrants, especially from South Korea and Taiwan, further eroded Japan's market share.

Japan's declining semiconductor industry has been closely linked to its inability to foster start-ups that could take advantage of the vertical disintegration model that transformed global semiconductor manufacturing (Motohashi, 2011, p.7). Compared to major competitors, Japan has long been considered 'inhospitable to high-tech start-up ventures' and has lagged in implementing policies that encourage innovation in the semiconductor sector (Brown and Linden, 2010, p.22; Motohashi, 2015, p.7; Kushida, 2023, p.2). This is partly due to Japan's institutions and practices that were a source of success in the 1970s and 1980s but had become to inhibit innovation and growth once Japan reached the technological frontier. For example, tradition of lifetime employment, which encourages long-term relationships and suppresses labour mobility, making it difficult for talent to leave established firms and join or create start-ups (Brown and Linden, 2010, p.36; Kushida, 2023, p.2).

For example, in 2004, Japan had more than 50 electronics companies with revenues exceeding US$1 billion, but all of these firms were established before 1968, highlighting the lack of new entrants (Brown and Linden, 2010, p.22). As Brown and Linden (2010, p.23) observe, new companies in Japan are often created as wholly-owned subsidiaries of large firms, rather than as independent start-ups, with technology and resources assigned from the parent company. Because these subsidiaries are protected from failure and often become involved in product development later in the process, they tend to weaker incentives and are rarely truly innovative organisations (Brown and Linden, 2010, p.23).

Japan initiated an EUV (extreme ultraviolet) lithography project in Tsukuba, where the government invested in the construction of a large, state-of-the-art cleanroom facility. Although leading Japanese equipment manufacturers, Canon and Nikon, eventually withdrew from the EUV lithography race—limiting the project's impact on Japan's competitiveness in stepper technology—the initiative proved highly significant for other segments of the EUV ecosystem. It played a critical role in advancing the capabilities of key materials suppliers, including EUV mask producers such as Hoya, Asahi Glass, and Dainippon Printing; photoresist manufacturers like JSR and Tokyo Ohka; and wafer suppliers such as Shin-Etsu. These firms remain integral to the global EUV supply chain today.

Ironically, adjacent to the original cleanroom facility in Tsukuba, TSMC now operates a major site that houses its manufacturing engineering group. This facility is reportedly staffed primarily by Japanese engineers—many of whom were formerly employed in Japan's semiconductor industry and were later recruited by TSMC—while management roles are typically held by personnel from Taiwan.

Innovation was also hampered by Japan's relatively slow embrace of industry–academia collaboration. In the United States, the Semiconductor Research Corporation ('SRC'), established in 1982, funded hundreds of research projects at universities and became a major driver of innovation (Sumney and Burger, 1987, p.39; Burger, 2000, pp.7-8). By contrast, Japan's Semiconductor Technology Academic Research Centre was not founded until 2005, reflecting a significant lag in institutional support for collaborative research (Motohashi, 2015, p.4; Lim, 2023, pp.48-49).

Current global situation

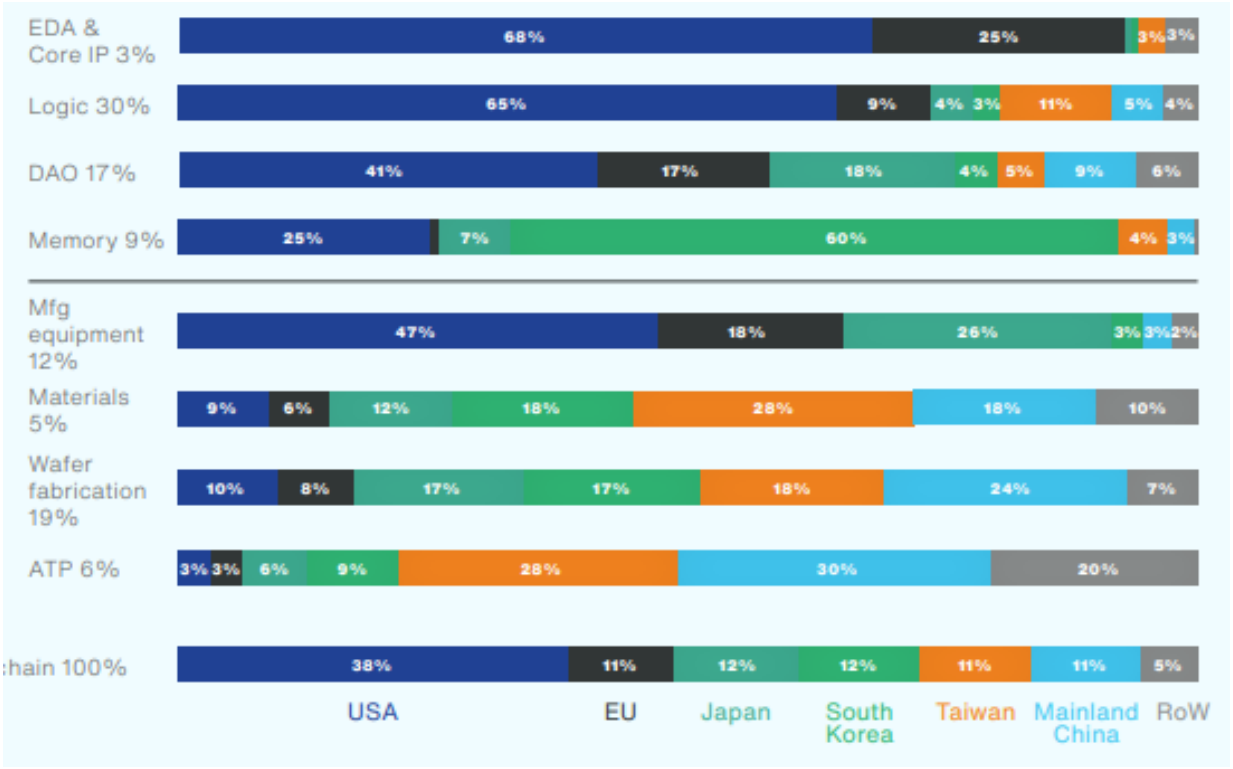
Figure 2 shows a breakdown of the chip value chain and the allocation of activities across economies. With respect to the first four lines of the figure, 'EDA' stands for Electronic Design Automation, which is specialised software that engineers use to design and test computer chips before they are manufactured. Core IP refers to core intellectual property, including reusable design elements or building blocks, such as central processing units or communication components, that chip designers frequently license rather than build from scratch. Logic represents semiconductor devices that process data and run instructions – they are critical for creating processors and other parts of electronic systems that actually 'think' or 'compute'. Lastly, 'DAO' is an acronym for Discretes, Analog, and Optoelectronics. This group includes basic semiconductor parts like transistors and diodes (discretes), chips that work with continuously varying signals (analog), and devices that interact with or control light such as LEDs and light sensors (optoelectronics)

According to Figure 2, the current situation of the global semiconductor supply chain is characterised by a high level of specialisation and regional concentration. Striking is the extent to which these activities take place in the Asia Pacific. More specifically:

- R&D and Design (lines 1-4): US-headquartered companies are dominant, leading in chip design, core intellectual property EDA.
- Equipment: The US, EU and Japan jointly lead in manufacturing equipment.
- Materials: Companies headquartered in China, Japan, Taiwan and South Korea lead in the supply of semiconductor materials.
- Wafer Fabrication: The most advanced manufacturing – especially for chips below 10 nanometers – is highly concentrated in South Korea and Taiwan.
- Assembly, Test, and Packaging (ATP): This segment is primarily based in China and Taiwan, with almost 60% of global ATP capacity located in these two places.

This structure has created efficiency and cost advantages by allowing each region to focus on what it does best. For instance, the US excels in design and core technology, while Asia is critical for advanced manufacturing and assembly. However, it also means the supply chain is vulnerable to disruptions – such as natural disasters, political instability or trade conflicts – because so much capacity is concentrated in a handful of countries.

Figure 2: Sources of value added by activity and economy, 2022 (%)



Source: Boston Consulting Group and Semiconductor Industry Association, 2024, p.10

Motivations for Government Intervention

The Japanese government's intervention since the early 2020s in the semiconductor sector has been driven by economic, technological and geopolitical considerations. The COVID-19 pandemic exposed vulnerabilities in global chip supply chains, leading to production stoppages in key industries such as automotive production, highlighting Japan's heavy reliance on imports, particularly from Taiwan (Huang, 2024; Koh, 2024, pp.80-81).

Geopolitical tensions, especially between the United States and China, the risk of conflict in East Asia and the weaponisation of economic interdependencies have led to more attention to the role of domestic semiconductor production (Solís and Duchâtel, 2024). Semiconductors are now viewed as critical infrastructure for national security, advanced manufacturing and defence. Japan's lag in advanced chip technology (operating at 40nm nodes versus 3-5nm globally) led to concerns about falling behind in AI, quantum computing and next-generation communications (Kamakura, 2022, p.267; Shivakumar, Wessner and Howell, 2023, p.4; Koh, 2024, p.79-80). These concerns are especially pronounced given Japan's historical context of having a long experience in chip production and once being a global leader. The Japanese government aims to recover assets from the country's past and remaining endowments in semiconductor equipment and materials to rebuild a competitive ecosystem (Koh, 2024, p.77).

The global industrial policy race – including the US CHIPS Act, the EU Chips Act and China's subsidies for domestic chip production – has created an environment where it is argued that state support is essential to compete (Access Partnership, 2022; Solís and Duchâtel, 2024).

Forms and Extent of Intervention

Japan's intervention includes several instruments including direct subsidies, tax incentives, R&D funding, public–private partnerships and international alliances (METI, 2024, pp.6-7; Koh, 2024, p.76). In total, government funding of over JPY3.9 trillion (US$27 billion) was allocated from 2021 to 2023, equivalent to 0.71 per cent of GDP – the highest among major economies relative to GDP (Negrine, 2024). Table 1 summarise the package of initiatives and more detail follows.

Table 1: Components of Japan's Semiconductor Industry Policy

Policy/Project	Description	Government Spending/Subsidy	Timeline	Expected Outcomes/Notes
Overall Government Spending	Comprehensive government support for the semiconductor industry (2021–2023)	JPY3.9T (US$27B)	2021–2023	Highest public semiconductor investment-to-GDP ratio (0.71%) among major economies
TSMC, Sony, Denso (JASM)	Joint venture for logic chip production in Kumamoto; two fabs (front-end manufacturing)	JPY476B (US$3.17B, 1st fab); JPY732B (US$4.88B, 2nd fab)	2021–2027	Over 100,000 wafers/month; >10,000 jobs; US$51B economic ripple between 2022–2031; 46+ related manufacturers in Kyushu
Kioxia & Western Digital	Joint venture for 3D NAND flash memory at Yokkaichi and Kitakami	JPY92.9B (Jul 2022); JPY150B (Feb 2024); total >US$1.6B	2022–2030	Mass production of 218-layer NAND (2025); aim for 1000-layer NAND by 2030
Micron	Advanced DRAM production in Hiroshima; includes EUV equipment	US$310M (Jul 2022); US$1.1B (Oct 2023); total >US$1.4B	By 2026	Subsidies cover ~40% of planned investment
Rapidus	Consortium of 8 Japanese firms for 2nm logic chips; Hokkaido plant	JPY920B (US$6B) since 2022; JPY200B (US$1.3B) proposed	2022–2027	Targeting mass production of 2nm chips by 2027; private investment low; project cost up to JPY5T (US$33B)

Leading-edge Semiconductor Technology Centre (LTSC)	R&D hub for next-gen technologies; global collaboration focus	Not specified	Established Dec 2022	Success depends on flexible goals and diverse firm participation
R&D (General)	METI support for next-gen semiconductors and photonics-electronics convergence	US$8.9B (2021–2023)	2021–2023	Includes back-end process R&D, energy-saving tech for data centres
Samsung R&D (Yokohama)	R&D centre for back-end process technologies	Up to US$140M (about half of project cost)	Ongoing	Part of broader R&D and technology convergence push
TSMC R&D (Tsukuba)	R&D centre for 3D chip integration technology	About half of JPY37B (US$239M) project	Ongoing	Collaboration with ~20 Japanese chipmakers; criticism over lack of IP rights for public funder

Source: Authors, based on original sources listed below.

TSMC/Sony/Denso's JASM Fabs in Kumamoto

The intervention includes substantial government support for the establishment and expansion of Taiwan Semiconductor Manufacturing Company's (TSMC) operations in Kumamoto Prefecture in Kyushu, under the Japan Advanced Semiconductor Manufacturing (JASM) joint venture with Sony and Denso, and more recently, Toyota (Access Partnership, 2022; METI, 2024, pp.6-7). The Japanese government committed up to JPY476 billion (approximately US$3.5 billion) in subsidies for the first JASM fab, which caters to various process technologies, including '40, 22/28, 12/16 and 6/7 nanometer' legacy chips for automotive, industrial and consumer electronics sectors (Ryugen, 2024; TSMC, 2024, p.1).

The first fab, with a total investment of $8.6 billion from TSMC, was scheduled to begin production by the end of 2024 and is expected – having revised its projections upward – to have a monthly capacity of 55,000 12-inch wafers (Access Partnership, 2022; Shen and Blanchard, 2022). News reports indicate this goal was achieved. Sony invested around US$500 million for a stake of less than 20 per cent, while Denso contributed US$350 million for over 10 per cent equity, reflecting their assessment of the strategic importance of securing chips for the digital transformation (TSMC, 2021, p.1; Denso, 2022). The project could respond to assessments of Japan's vulnerability to global supply chain disruptions, particularly for chips needed in automotive and industrial applications, and to strengthen the domestic ecosystem by attracting a network of suppliers and related investments to the Kyushu region (Huang, 2024; Solís and Duchâtel, 2024).

Following what was regarded as the rapid progress and success of the first fab, a second JASM fab was announced in February 2024, with Toyota joining as an additional investor. The second fab, supported by up to JPY732 billion (about US$4.9 billion) in government subsidies, will produce more advanced chips down to the

6nm node, with operations expected to begin by the end of 2027 (Denso, 2024; METI, 2024, p.7; TSMC, 2024, p.1). The combined investment for both fabs will exceed $20 billion, making it one of the largest semiconductor projects in Japan's history (TSMC, 2024, p.1).

The economic impact of the JASM project is significant. According to estimates by Kyushu Financial Group, it is expected to create over 10,000 jobs in the region (METI, 2024, p.8). Other reports indicate that the project has catalysed a wave of 10s of billions in US$ terms of semiconductor-related investments in Kyushu since 2021. The government's strategy of subsidising up to one-third of capital costs, conditional on long-term domestic production and prioritisation of domestic shipments during shortages, was a significant factor in attracting TSMC and its partners (Shivakumar, Wessner and Howell, 2023, p.3; METI, 2024, p.5).

The JASM project's execution appeared relatively fast: construction began in April 2022 and the first facility opened in February 2024, a timeline that contrasted sharply with delays that were experienced by similar projects in the United States – namely, the fully-TSMC-owned fabrication plants in Arizona (Huang, 2024). The presence of TSMC has also encouraged Japanese suppliers, such as Sumco (silicon wafers), Tokyo Electron (equipment) and other materials and component manufacturers, to expand operations in Kyushu, reinforcing the region's reputation as 'Silicon Island' (Chiang and Hsiao, 2024; Satoh and Ting-Fang, 2024; Solís and Duchâtel, 2024). Unlike the Kumamoto fab, the Arizona fab produces more advanced chips (between 3–5nm) and has secured steady demand from key clients like AMD, Apple and NVIDIA (Priyadarshi, 2025). That has allowed the US-based fab to quickly achieve profitability. Meanwhile, expansions of the Kumamoto fabs have lagged due to weak investment and consumer demand, as well as competition in the market for legacy chips, having a dampening effect on facility utilisation.

Rapidus in Hokkaido

In parallel with the JASM initiative, the Japanese government has made a larger wager on Rapidus: a new domestic foundry established in Hokkaido with the goal of leapfrogging to 2nm logic chip production by 2027 (Grant-Chapman and McGee, 2024; METI, 2024, p.15; Chang, 2025). Rapidus is backed by a consortium of eight major Japanese companies – Toyota, Sony, Denso, Kioxia, NEC, NTT, SoftBank, and Mitsubishi UFJ – and is supported by extensive government funding. As of July 2025, the government had already allocated at least JPY1.72 trillion (over US$11.4 billion) in subsidies to Rapidus, with additional funding being considered to secure veto power over management decisions (METI, 2024, p.15; TrendForce, 2025). Hokkaido's water resources, cool climate and renewable energy potential have advantages for chip manufacturing (JETRO, 2025).

What distinguishes Rapidus from earlier consortia attempts like the VLSI is its commercial focus on frontier technologies. As described above, the VLSI effectively functioned as a government–industry research program, bringing together Japanese firms that were already competitive and seeking to improve domestic knowledge. In comparison, Rapidus is seeking commercial viability in advanced logic chip manufacturing – where it lacks an existent manufacturing base – leveraging international partnerships within a vastly more globalised supply chain.

The project's ambition is to skip multiple generations of semiconductor technology, moving directly from Japan's current 40nm capabilities to the 2nm node – an unprecedented technological leap (Shivakumar, Wessner and Howell, 2023, p.4; Chang, 2025). Rapidus has established strategic partnerships with IBM, which developed the world's first 2nm process technology, and with IMEC, Europe's leading nanoelectronics R&D centre (IMEC, 2023; Shivakumar, Wessner and Howell, 2023, pp.4-5; METI, 2024, p.15). More than 100 Rapidus engineers have been dispatched to IBM's Albany research facility in New York to accelerate technology transfer and skill development (Koh, 2024, p.78; METI, 2024, p.15).

Construction of the pilot line in Chitose, Hokkaido, began in late 2023, with equipment installation and test runs scheduled for 2025. The facility will employ advanced extreme ultraviolet (EUV) lithography and is designed to serve as a rapid-turnaround foundry for specialised, high-value chips, targeting applications in AI, data centres and next-generation communications (METI, 2024, p.15; TechPowerUp, 2025). Rapidus's business model of 'hot lots' differs from TSMC's mass production approach; it aims to deliver smaller batches of custom chips with fast turnaround times, appealing to customers who require specialised solutions and value supply chain resilience (Grant-Chapman and McGee, 2024; Chang, 2025).

The total investment required for mass production is estimated at around JPY5 trillion (over US$32 billion) and, as of mid-2025, most of the funding has come from the government, with private sector contributions remaining modest (Kyodo News, 2025). Rapidus is actively seeking additional private investment and bank loans and is expected to request further capital from its consortium members (Sumikawa, 2025). The project's success will depend not only on technological execution but also on its ability to attract customers willing to redesign chips for a new, unproven foundry, and on building a skilled workforce in a country facing acute engineering shortages (Grant-Chapman and McGee, 2024; Koh, 2024, p.80; Satoh and Ting-Fang, 2024). To succeed, Rapidus will need a major customer – like Qualcom, Broadcom or NVIDIA – that has volume and has a team that is able to work with Rapidus to bring them up the learning curve to the frontier.

Other Significant Investments and Regional Clusters

Beyond the headline projects in Kumamoto and Hokkaido, the Japanese government has extended substantial subsidies to other major semiconductor manufacturers. Kioxia and Western Digital's joint venture facilities in the Mie and Iwate prefectures will receive up to JPY243 billion (about US$1.62 billion) to support the production of advanced 3D NAND flash memory (METI, 2024, p.7; Nikkei Asia, 2024). Micron's Hiroshima operations have been awarded JPY46.5 billion (about US$320 million) to help bring EUV lithography and next-generation DRAM technology to Japan (METI, 2024, p.6). Sony is also expanding sensor production in Kyushu, further strengthening the regional ecosystem (Solís and Duchâtel, 2024).

These investments are part of a broader strategy to develop semiconductor manufacturing clusters in key regions: Kumamoto (Kyushu), Hokkaido, Mie (Chubu), and Hiroshima (Chugoku). Each cluster benefits from targeted government support, partnerships with local universities for workforce development and the attraction

of suppliers and related industries (METI, 2024, p.20; Solís and Duchâtel, 2024). For example, Kyushu has seen more than 100 chip-related investments since 2021, with over 200 semiconductor-related companies now operating in Kumamoto alone (Brown, 2024; Kyushu Bureau of Economy, Trade and Industry, 2024, p.10).

R&D and human capital development are central to the strategy, with the establishment of the Leading-Edge Semiconductor Technology Centre ('LSTC') for collaborative R&D and talent development, and regional consortia in Kyushu, Hokkaido, Chubu, Tohoku, Chugoku and Kanto focusing on workforce training and curriculum development (METI, 2024, p.20; Koh, 2024, p.78).

While less prominent in the initial phase of Japan's chip revival, tax incentives are becoming increasingly important as a tool for sustaining investment, supporting ongoing production and encouraging broader participation from both domestic and foreign firms. Recent policy reforms have introduced a 10-year corporate tax reduction for companies investing in strategic sectors, including semiconductors, with the possibility of a 20 per cent annual reduction in corporate tax liability for eligible semiconductor investments (PwC, 2025). These incentives are designed to lower the ongoing cost of production, encourage expansion and make Japan more competitive with other jurisdictions offering similar benefits, such as the US CHIPS Act and the EU Chips Act (Grant-Chapman and McGee, 2024).

Tax incentives are particularly valuable for promoting incremental investment, supporting the scaling of existing facilities and encouraging R&D and innovation activities. They are also structured to reward companies based on production and sales volumes, aligning support with actual economic performance and market creation (METI, 2024, p.12). In addition, Japan has introduced 'innovation box' tax incentives to attract R&D centres and support the commercialisation of patents and copyrights related to semiconductor technology (C-ITS, 2024).

Assessments of Progress

The JASM project in Kumamoto is widely regarded as making good progress, having met construction and production milestones faster than comparable projects in the United States thanks to streamlined government support, flexible labour practices and strong local partnerships (Huang, 2024). The project has catalysed extensive investment in local supply chains and infrastructure (Chiang and Hsiao, 2024).

Rapidus, on the other hand, is seen as a high-risk, high-reward initiative. While significant progress has been made in R&D, construction and talent development, major challenges remain in scaling up to 2nm production, securing sufficient private investment and attracting customers (Shivakumar, Wessner and Howell, 2023, p.5; Grant-Chapman and McGee, 2024; METI, 2024, p.13). The technological leap from 40nm to 2nm is unprecedented and fraught with risk (Chang, 2025).

Workforce and ecosystem development efforts are making headway, particularly through regional consortia and academic partnerships. However, the overall talent shortage remains acute, with the aging workforce, declining STEM enrolment and limited immigration policies posing significant challenges (Koh, 2024, p.80; Grant-Chapman and McGee, 2024).

Private investment has been successfully leveraged in the case of JASM, but less so for Rapidus, where consortium members' capital commitments remain limited compared to the scale of government funding (Koh, 2024, p.80; Solís and Duchâtel, 2024).

Regional Context

Jeong (2025) has reported on developments in the chip industry in the region, utilising the Trade Specialization Index ('TSI') and Revealed Symmetric Comparative Advantage ('RSCA') to analyse the semiconductor competitiveness of major economies. These metrics reveal important trends for both memory and system semiconductors.

For memory semiconductors, Jeong finds that Korea has traditionally maintained a strong comparative advantage, reflected in consistently high TSI and RSCA values and a significant trade surplus. However, these indicators have plateaued or declined in recent years, signalling an erosion of Korea's edge. This trend is attributed to the rapid technological progress and state-backed investment in China, with firms such as CXMT and YMTC achieving mass production of advanced DRAM and NAND flash. China's RSCA for memory semiconductors has shown a clear upward trajectory, indicating a growing comparative advantage, although its TSI remains negative, showing it is not yet a net exporter (Jeong, 2025, p.10). The United States, with companies like Micron and SanDisk, is closing the technology gap with Korea, supported by robust patent portfolios and industrial policy. Taiwan's role in memory semiconductors is less pronounced, as it focuses more on system chips and foundry services, though it remains a key partner in packaging and assembly.

Japan, meanwhile, is moving towards greater supply chain independence in memory chips, supported by domestic production (such as Micron Japan) and innovation from companies like Kioxia. Japan's new chip policy (discussed above) could strengthen its position in memory semiconductors and reduce reliance on imports.

In the field of system semiconductors (logic chips plus other system drivers), Jeong (2025, p.17) finds that Taiwan leads in competitiveness, consistently recording the highest TSI and RSCA values, underpinned by TSMC's global dominance in foundry services and advanced process nodes. The United States is also a leader in system chips, particularly in advanced segments such as AI and high-performance computing, with companies like Intel, Qualcomm and NVIDIA (a global leader in AI chips and GPU design) driving innovation and patent leadership. Korea's competitiveness in system semiconductors is positive but has stagnated, with the gap

widening relative to Taiwan and the United States. China's indices for system semiconductors are still low, but upward trends reflect rapid expansion in legacy and mid-tier chips (Bown and Wang, 2024, p.97), supported by state-led investment and domestic foundry growth.

Japan's competitiveness in system semiconductors is moderate but improving. This trend could be supported by the new government policies supporting advanced logic chip production and partnerships with TSMC and other global leaders. Japan's new chip policy, with its focus on attracting advanced manufacturing and deepening collaboration with global fabless leaders, is designed to restore competitiveness in advanced nodes and AI chips.

Prospects and Key Risks

The previous section indicates that Japan could reclaim a significant role in the global semiconductor ecosystem, particularly in equipment, materials and specialised logic/memory chips for automotive, industrial and AI applications (see also Koh, 2024, p.77; Solís and Duchâtel, 2024). The JASM model of international collaboration, public–private partnerships and targeted subsidies in rapidly scaling up manufacturing capabilities could succeed (Huang, 2024; METI, 2024, p.8). If successful, Rapidus could improve the position of Japan among advanced chip producers, with implications for AI, quantum computing and national security (Nishimura, 2022; METI, 2024, p.10).

We have detailed Japan's earlier problems in the semiconductor industry as including over-coordination, excessive standardisation and a lack of competition, which led to reduced innovation, slow adaptation to global trends and ultimately a loss of market share (Tomoshige, 2022; Grant-Chapman and McGee, 2024). In the 1970s and 1980s, government-led projects like the VLSI attempted to foster collaboration and rapid technological progress. But over time, these joint efforts resulted in a homogenised industrial structure where companies failed to specialise and had standardised technologies, reducing diversity and the ability to respond flexibly to new market demands (Tomoshige, 2022). And attempts at 'all-Japan' approaches – such as joint foundries and consortia – often failed because 'companies were reluctant to share key personnel and proprietary knowledge', and because these efforts stifled internal competition (Tomoshige, 2022; Suzuki, 2025). Further, large electronics companies that had a diverse product range struggled to devote the resources necessary for ongoing capital investments in semiconductor developments (Suzuki, 2025). The new policy framework manages these risks in several ways:

Emphasis on International Partnerships and Openness:

Unlike earlier inward-looking strategies, the current policy actively invites foreign firms – most notably TSMC – to establish manufacturing in Japan, with the government subsidising up to half of construction costs and supporting joint ventures with Japanese companies (Access Partnership, 2022; METI, 2024, p.3). This approach introduces new technology, global best practices and external competition directly into the Japanese ecosystem,

countering the risk of insularity and over-standardisation (Shivakumar, Wessner and Howell, 2023, p.3; Chang, 2025).

Diversification of Industry Players and Business Models:

Rather than consolidating all resources into a single 'national champion', Japan's new strategy supports a mix of both foreign-led (TSMC/JASM) and domestic-led (Rapidus) projects, each with different business models and technological focuses (Solís and Duchâtel, 2024; Chang, 2025). This hedging reduces the risk of systemic failure and encourages competition between different approaches, fostering innovation and adaptability.

Market-Driven and Technology-Driven Collaboration:

The government is now more focused on unlocking private investment and ensuring that public support is tied to compelling business and technological rationales. For example, the justification of TSMC's Kumamoto project was linked to a business case involving Sony's demand for advanced image sensors (Solís and Duchâtel, 2024). This market-driven approach contrasts with past efforts that were often driven solely by government direction and resulted in duplicative or misaligned investments (Tomoshige, 2022).

Flexible, Modular Coordination Structures:

Institutions like the LSTC are designed as open, collaborative platforms that bring together academia, industry and international partners for R&D and workforce development, rather than imposing rigid, top-down coordination (Shivakumar, Wessner and Howell, 2023, p.4; Grant-Chapman and McGee, 2024). This structure allows for more diverse input and aims to avoid the pitfalls of over-centralisation.

Incentives for Diversity and Innovation:

Policy tools such as R&D tax credits, targeted subsidies and support for regional clusters are used to encourage risk-taking, diversification of research paths and the development of new business models, rather than enforcing a single technological standard or approach (Grant-Chapman and McGee, 2024).

Learning from Past Failures:

Japanese policymakers have explicitly acknowledged the failures of previous over-coordinated, standardised approaches and are now prioritising strategic autonomy, openness and the integration of global expertise (Chang, 2025; Suzuki, 2025). The willingness to support foreign-led projects and to facilitate international R&D collaborations marks a clear break from the 'all-Japan' mentality of the past (Shivakumar, Wessner and Howell, 2023, p.3).

Japan has ongoing dependence on foreign sources for critical raw materials (such as silicon wafers, rare earths and specialty chemicals) and the practice of sending semiconductor wafers abroad for assembly, test and packaging (ATP) before re-importing the finished chips. These aspects are both a normal part of the global semiconductor value chain and a source of risk for Japan. Globally, the semiconductor industry is highly

specialised and geographically distributed. It is common for raw materials, wafer fabrication and ATP to occur in different countries, to capture cost advantages, expertise, and economies of scale.

Japan, like many advanced economies, excels in front-end manufacturing (wafer fabrication) and the supply of materials and equipment, but other parts of the production process are often outsourced to specialised firms in other countries, primarily in Taiwan, which is the global leader in outsourced semiconductor assembly and test (OSAT) services (Tung, 2023, p.34; Koh, 2024, p.81). This arrangement allows Japanese firms to benefit from cost efficiencies and the advanced capabilities of these overseas providers.

However, this reliance also introduces several risks. First, it exposes Japan to potential supply chain disruptions caused by geopolitical tensions, natural disasters, or trade restrictions, particularly given the concentration of ATP capacity in Taiwan and, for some commodity chips, in China (Tung, 2023, pp.23-25; Koh, 2024, p.78; Solís and Duchâtel, 2024). Second, it raises national security concerns, as semiconductors are critical to Japan's economy and defence, and dependence on foreign ATP providers – especially in regions with which Japan has strategic tensions – could make the country vulnerable to embargoes or politically motivated supply interruptions. Third, it limits Japan's control over quality, turnaround times and intellectual property protection, which are especially important for advanced or sensitive applications.

Japanese companies cannot compete globally if it is not integrated into global semiconductor value chains. Dependence on foreign countries creates vulnerabilities to external shocks and reduces economic and strategic resilience but that has to be managed alongside the risks that become concentrated with further onshoring or reliance on manufacturing in Japan. This is one reason that Japanese industrial policy places a strong emphasis on supply chain security (Koh, 2024, p.78; METI, 2024, p.5; Solís and Duchâtel, 2024).

In addition, the attempt to jump directly from manufacturing 40nm to 2nm chips is unprecedented and failure could result in wasted investment and reputational damage (Shivakumar, Wessner and Howell, 2023, pp.4-5; Chang, 2025). Rapidus's funding remains far short of the estimated JPY5 trillion needed for mass production, with private sector partners contributing only a fraction of the total (Koh, 2024, p.80; METI, 2024, p.15).

Compounding these challenges are the talent shortage and relatively high utility costs, as well as intensifying global competition, with countries like India and Vietnam ramping up their own semiconductor ambitions. A global subsidy race – especially in an attempt to push out the technological frontier – could lead to spiralling inefficiencies and resource misallocation (Koh, 2024, p.79; Negrine, 2024).

Analysis of Costs and Benefits

The cost-benefit analyses undertaken by Japan's new semiconductor policy are primarily documented in government, industry and academic reports, with some input from independent consultancies. However, most detailed economic impact assessments have been either commissioned by, or closely coordinated with, stakeholders involved in the major projects (Huang and Lin, 2024; METI, 2024, pp.8-9).

For the TSMC/Sony/Denso JASM fabs in Kumamoto, the Ministry of Economy, Trade and Industry ('METI') and local authorities have presented several analyses of the expected economic impact. The Kyushu Financial Group, for example, estimated that the economic ripple effect of the JASM investment over ten years would be about US$51 billion, including the creation of approximately 10,700 jobs and the development of around 90 new facilities in Kumamoto Prefecture (METI, 2024, p.8). These estimates are based on standard input-output and computable general equilibrium (CGE) modelling, which are widely used for such assessments and are described as 'increasingly being adopted internationally' (METI, 2024, p.9).

Analyses are either commissioned by METI, local government or industry groups, and the models rely on data and assumptions provided by project stakeholders and media reports (METI, 2024, p.8). The direct beneficiaries – TSMC, Sony, Denso and local suppliers – have also contributed information and projections. Independent, peer-reviewed cost-benefit analyses conducted by a third party without ties to the government or industry are best practice. Further, as Bown and Wang (2024, p.102) point out, evaluating the impact of government interventions 'must now account for not only direct subsidies, but also the near simultaneous imposition of export controls, import tariffs, foreign investment screening, and sometimes antitrust actions'.

For the Rapidus project in Hokkaido, the available cost-benefit analysis is less detailed and more speculative. Government projections cite the expected economic and strategic benefits of developing domestic 2nm chip production, such as technological sovereignty, supply chain resilience and future growth in advanced manufacturing sectors (METI, 2024, p.3). The government has committed over JPY1 trillion in direct subsidies, with additional support for R&D, infrastructure and workforce development (METI, 2024, p.15; Grant-Chapman and McGee, 2024). While some media and consultancy reports have cited government projections of a potential JPY1.04 trillion economic impact, these figures are not based on independent, published methodologies and are typically quoted from government or industry press releases.

The METI strategy documents and presentations provide detailed breakdowns of subsidy amounts, expected job creation and economic effects in other sectors, but these are again based on internal or commissioned modelling, not on independent academic or third-party evaluations (METI, 2024, pp.8-9). There do not appear to be external, arms-length cost-benefit analyses for Rapidus that are independent of the interests involved.

Japan's policy approach is justified in official documents by reference to international comparisons (e.g., Japan's 0.71 per cent of GDP in subsidies versus 0.2 per cent in the United States and 0.4 per cent in Germany) and by

the argument that the strategic and economic benefits of domestic chip production outweigh the costs (Huang, 2024; Solís and Duchâtel, 2024). The METI and government analyses emphasise not only direct economic returns but also national security, supply chain resilience and innovation spillovers – benefits that are inherently difficult to quantify and often not captured in traditional cost-benefit frameworks. Indeed, the weight of existing evidence indicates that industrial policy at the technological frontier – where spillover benefits are likely to be created – is less likely to be successful than industrial policy uses in developing countries that are importing and catching up to frontier technologies (Armstrong, Solís and Urata, 2025, pp.271-272).

One of the lessons for industrial policy is the importance of unlocking private investment and ensuring a compelling business and technology case, but the ultimate commercial viability and broader economic impact of these projects remain to be tested in practice (Solís and Duchâtel, 2024).

Conclusion – Lessons for Industry Policy

Japan's experience offers several lessons for industry policy. One key conclusion from its recent experience is the value of undertaking independent cost benefit analyses of interventions. This could additionally benefit from a mechanism for transparent monitoring and public reporting on the progress of projects.

Furthermore, there is value in considering how funding mechanisms can be linked to results (at the project level and in terms of local impact). This is a central challenge for governments aiming to maximise the impact of public investment and avoid wasteful or ineffective support. In the context of Japan's new semiconductor strategy, both direct subsidies and tax incentives are used, but their effectiveness and the ways they can be tied to measurable outcomes differ (Criscuolo et al., 2022, p.20).

Japan's approach to direct subsidies increasingly incorporates conditions and performance milestones to ensure that funding leads to tangible outcomes. For example, subsidies for major projects like TSMC's JASM fab and Rapidus are tied to requirements such as maintaining domestic production for a minimum period, prioritising domestic supply during shortages and achieving specific technological or production targets such as 2 nm chips (Shivakumar, Wessner and Howell, 2023, p.3; Chiang and Lin, 2024). This model is designed to ensure that public money results in increased domestic capacity, technology transfer and job creation rather than simply subsidising private profit (Grant-Chapman and McGee, 2024; Armstrong, Solís and Urata, 2025, p.271). Such local content requirements and restrictions tied to domestic demand are likely to inhibit competitiveness. The key test for industrial policy is the international market test: JASM and Rapidus must be competitive in international markets. Any distortions that hinder that will make success less likely.

Best practice, as highlighted in international literature, also recommends using matched funding (requiring private sector co-investment), staged disbursement based on project milestones and regular evaluation of progress against clear key performance indicators (Industry Innovation and Science Australia, 2022, p.25). At

the time of writing, the Japanese government has not made further public funding for Rapidus contingent on increased private sector investment, but rather has conditioned further funding on receiving voting rights (TrendForce, 2025).

Tax incentives, such as R&D tax credits or production-based tax reductions, are generally less prescriptive and more market-driven than direct subsidies. They reward companies for actual investment, production or R&D activity, rather than for submitting successful grant applications. This means that support is only delivered if companies undertake the desired activity, providing a natural link between funding and results (Criscuolo et al., 2022, pp.10-11; Grant-Chapman and McGee, 2024).

Tax incentives satisfy the desideratum of competition-neutrality, with lower administrative costs and less risk of political capture or favouritism (Criscuolo et al., 2022, p.27). They also provide continuous support, encouraging long-term investment and innovation, and allow firms to choose projects based on market signals rather than government selection. However, there is a risk that some tax-incentivised activity would have happened anyway and it can be harder to target support to specific sectors or national priorities (OECD, 2024, p.11).

In summary, Japanese industrial policy can reduce risks by adopting best practice. At the broadest level, industrial policy must be underpinned by a compelling business and technology case, with projects that align with market needs and leverage local strengths more likely to succeed (Solís and Duchâtel, 2024). Japan's strengths in materials and equipment based on its history in the chip sector provide a foundation for revival (Koh, 2024, p.77; Solís and Duchâtel, 2024). While a clearly defined market is important, strategic flexibility – as seen in Japan's dual-track approach of backing both high-risk (Rapidus) and lower-risk (JASM) projects – allows for adaptive learning and hedges against uncertainty (Solís and Duchâtel, 2024). Building a robust ecosystem – including equipment, materials, design, manufacturing, and packaging – is valuable for long-term competitiveness. Dasher et al. (2015, p.7) suggest eleven constitutive factors spanning finance, human capital, industry–university–government collaboration, industrial organisation, entrepreneurship culture and business infrastructure. Regional consortia and collaboration with universities are promising, but broader immigration reform may be needed to address acute shortages (Koh, 2024, p.81; Grant-Chapman and McGee, 2024; METI, 2024, p.20).

State subsidies are most effective when they catalyse significant private-sector commitment in capital-intensive sectors, as demonstrated by the JASM project (Solís and Duchâtel, 2024). Indeed, subsidies are preferred for high-risk, high-impact projects where the government wants to accelerate specific technologies, attract foreign investment or overcome market failures that the private sector alone would not address (Kleer, 2010, pp.1361-1362; Svensson, 2024; p.293). To avoid spiralling government costs, subsidies should be tightly linked to measurable milestones and private co-investment. Meanwhile, tax incentives are generally preferred for encouraging broad-based, incremental investment and innovation across the economy, supporting a wider range of firms and reducing bureaucratic overhead (Criscuolo et al., 2022; Svensson, 2024, p.292).

Empirical studies show that both subsidies and tax incentives can stimulate R&D and innovation, but tax incentives are more competition-neutral and continuous, while targeted subsidies are better for projects with long lead times, high uncertainty or major spillovers (Svensson, 2024, p.292). In either case, it is critical to regularly review and adjust both tools based on independent evaluation of outcomes and evolving industry needs (Criscuolo et al., 2022; OECD, 2024).

Finally, it is worth underscoring that industrial policy need not be an island. International collaboration has facilitated the shift in competitiveness, accelerating technology transfer and reducing risks associated with research and development (Shivakumar, Wessner and Howell, 2023, p.7; METI, 2024, p.22). Cooperation and transparency can be used to manage the risk of subsidy wars and foster international R&D and contribute to supply chain resilience (Shivakumar, Wessner and Howell, 2023; METI, 2024, p.22). The multilateral agencies observe that (IMF, OECD, World Bank and WTO, 2022, p. vii))

> "....international cooperation that delivers improved subsidy disciplines, improves business certainty, and reduces trade frictions would be superior to unilateral actions and should be expected to reduce their use. In many of these areas, better information, more extensive objective analysis, and regular dialogue can help governments accelerate reform of their own subsidies and expedite negotiations toward improved international disciplines"

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