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**Moore's Law, Increasing Complexity,
and the Limits of Organization:
The Modern Significance of Japanese Chipmakers' DRAM Business**

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Abstract:

The purpose of this paper is to identify the organizational constraints on science innovations in the midst of a bifurcating tendency between knowledge conception and implementation due to the increasing complexity of technology and markets. For this purpose, we scrutinize the rise and fall of Japanese chipmakers in their commodity DRAM business during the last three decades, during which time all of them have been deeply wounded. We take up this business case mainly because the Japanese semiconductor industry seems to be a forerunner of various science-based industries facing rapid globalization and could provide instructive examples for them in an age of speed-to-market. We think that the rise and fall of Japanese chipmakers in their commodity DRAM business has been deeply influenced by three kinds of ever-growing complexities: the growing market-complexity triggered by the collapse of commodity DRAM prices in 1996, the growing (manufacturing) system-complexity boosted by the advent of 200mm fabrication plants (fabs) in the early 1990s, and the growing process-complexity in fabrication technologies necessitated by 64Mb commodity DRAMs. We explain how and why, compared with U.S. and Korean competitors, Japanese chipmakers could not respond to these growing complexities in a systematic and well-organized manner.

**Moore's Law,¹ Increasing Complexity, and the Limits of Organization:
The Modern Significance of Japanese Chipmakers' Commodity DRAM Business²**

Hiroyuki Chuma³ and Norikazu Hashimoto⁴

1. Introduction

There has been a mounting interest in innovations which are defined here as ingenious inventions, discoveries, or improvements that could lead to significant changes in people's social life through markets. Such an interest is especially pronounced for innovations in various fields of science and technology induced mainly by science-based industries (referred to as "science innovations"). Indeed, the complexity of technologies and markets has been increasing so rapidly that it is extremely difficult to effectively implement science innovations. This tendency is further accelerating because of the globalization of various markets and consumers' diversified and upgraded preferences brought on by affluence.

Pari passu with the ever-growing complexity of technologies and markets, there has emerged a bifurcating tendency in knowledge creation/integration (or conception) and knowledge utilization (or implementation). Indeed, along with the created knowledge's increasing complexity, and the expertise required to understand it, it is extremely difficult to effectively and promptly implement such knowledge.

Consequently, as is clearly exemplified by the worldwide prevalence of the "Reference Design"⁵ approach in the semiconductor industry, both the high speed and new methods of knowledge implementation are crucial contributing factors for innovations. Indeed, the so-called "accelerating-network property" (Mattick and Gagen 2005) shows up beyond a certain threshold in complexity mainly because the total number of connections among nodes (methods of knowledge implementation) scales faster than the total number of nodes themselves (a body of created knowledge).⁶

¹ The experiential law predicted by Moore (1965): the number of transistors on integrated circuits doubles every two years. The historical background and origin of Moore's Law is described in Lojek (2007). DRAM is the abbreviation for Dynamic Random Access Memory.

² In writing this paper, we received much good advice from many semiconductor research scientists and engineers. Among them, we would like to express our special thanks to Professor Hideo Sunami (Research Center for Nanodevices and Systems, Hiroshima University), Dr. Kiyoo Itoh (Central Research Laboratory, Hitachi Ltd. Fellow), Dr. Katsuhiro Shimohigashi (STARC, CEO), and Dr. Hideaki Khozu (former chief engineer of NEC). We also are indebted to Mr. Toshiaki Fukano (visiting research assistant, Hitotsubashi University), who has excellent script language skills. Of course, all responsibility for any errors belongs to the authors.

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⁴ Former research director of Hitachi Central Research Laboratory.

⁵ The term "reference design" applies to a wide range of materials available to educate engineers and accelerate design cycles. For details, see the recent *ElectronicNews* article (<http://www.edn.com/article/CA6495302.html?nid=3351&rid=608686253>).

⁶ "Papert's Principle," *a la* Minsky below, also is closely related to the accelerating-network property: "Some of the most crucial steps in mental growth are based not simply on acquiring new skills, but on acquiring new administrative ways to use what one already knows" (Minsky 1986: 102 and Minsky 2006: 212).

The purpose of this paper is to identify the organizational constraints on science innovations in the midst of the bifurcating tendency between knowledge conception and implementation due to increasing complexity of technology and markets. For this purpose, we scrutinize the rise and fall of Japanese chipmakers in their commodity DRAM business during the last three decades, during which time all of them have been deeply wounded. We take up this business case mainly because the Japanese chipmakers seem to be a forerunner of various science-based industries facing ever-growing complexity in technology and markets and could provide instructive examples for them in an age of speed-to-market.

Indeed, under strong political pressure from the Japan-United States Semiconductor Trade Agreement (J_USTA),⁷ Japanese chipmakers had secured more than 70% of the world market share in commodity DRAMs until around 1990. After that, however, the share radically declined and is now around 10%. Despite such a weakening competitiveness, Japanese chipmakers have been proud of their leading-edge DRAM technologies, at least from 256 Kb(it) DRAM. Even today, their technological advantages remain and have been applied to various embedded as well as commodity DRAMs.

For 64Mb or larger DRAMs (more evidently 128Mb), however, Samsung Electronics in South Korea has been enjoying both pioneers' gains and mass production benefits, while for 16Mb or larger DRAMs, Micron Technology in the United States has experienced mass production benefits based on its superlative chip⁸-shrink technology. Moreover, since the mid-1990s, Japanese chipmakers have started to lose their comparative advantage even in the manufacturing system. Eventually all of the Japanese chipmakers retreated from the market one after another: Fujitsu in 1998, the Hitachi-NEC joint venture (Elpida) in 1999, Toshiba in 2001, and Mitsubishi in 2002.

We think that the rise and fall of Japanese chipmakers in their commodity DRAM business has been deeply influenced by three kinds of ever-growing complexities: the growing market-complexity triggered by the collapse of commodity DRAM prices in 1996, the growing (manufacturing) system-complexity boosted by the advent of 200mm fabrication plants (fabs) in the early 1990s, and the growing process-complexity in fabrication technologies necessitated by 64Mb commodity DRAMs.⁹ We explain how and why, compared with U.S. and Korean competitors, Japanese chipmakers could not respond to these growing complexities in a systematic

⁷ It was effective from July 1986 to April 1996.

⁸ Each tiny piece in a wafer is called a "chip."

⁹ Although 16Mb DRAM presaged them, complexities in process technologies and their integration drastically increased together with 64Mb DRAM. This is closely related to the DRAM-specific constraint that the minimum electric charge to be stored within each capacitor (called "storage capacitance") must be almost constant even when the chip-size tends to be miniaturized following Moore's law. For miniaturization, the external power supply (V_{dd}) to chip had to be also reduced to 3.3 V for 64Mb DRAM, while V_{dd} had been 5.0 V from 64Kb to 16Mb DRAMs (Itoh 2001, p.101). Moreover, several structural changes in basic circuit design such as a "hierarchical word-line structure" had to be newly introduced to avoid "Resistive Capacitive (RC) delay" from 64Mb DRAM (Itoh 2001, p.101 and p.141).

and well-organized manner.

2. Stylized Facts (SFs) about Japanese Chipmakers' Commodity DRAM Business

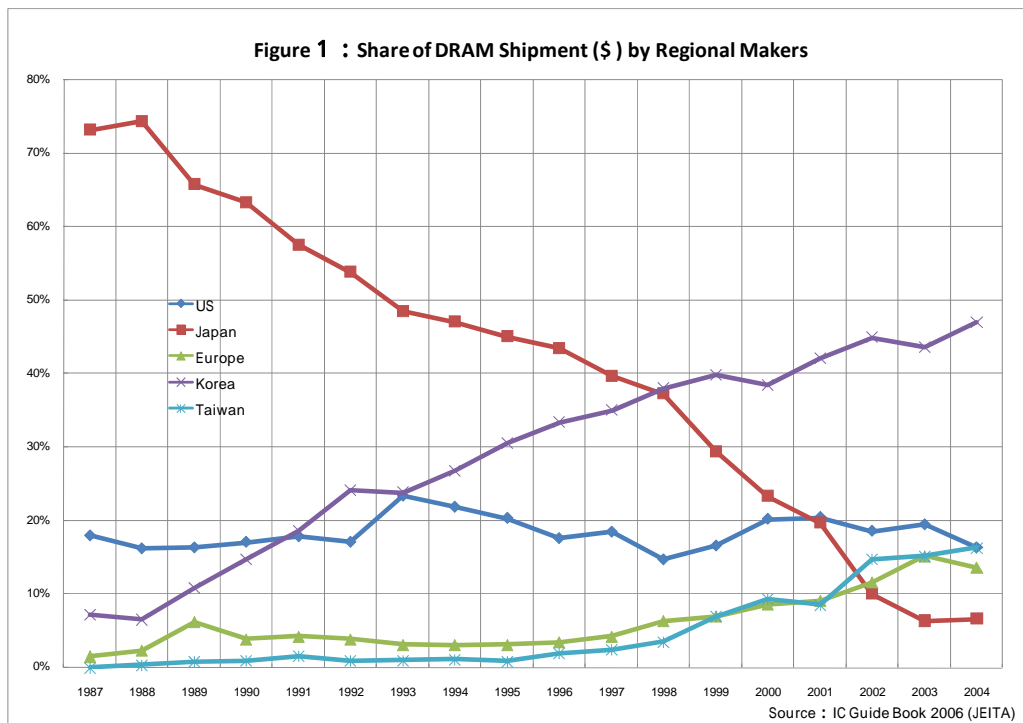
In this section, we first confirm the aforementioned SFs by using various hard evidences:

(SF1) Japanese chipmakers secured more than 70% of the world market share in commodity DRAMs until around 1990, but after that the share radically declined and is now around 10%.

(SF2) Japanese chipmakers have been proud of their leading-edge technologies in DRAM design and processing, at least from 256Kb DRAM. Even today, their technological advantages remain and have been applied to various embedded, as well as commodity DRAMs.

(SF3) For 64Mb or larger DRAMs (more evidently 128Mb), Samsung in South Korea has been enjoying both first mover's (pioneer's) gains and mass production benefits, while for 16Mb or larger DRAMs, Micron Technology in the United States has been experiencing mass production benefits based on its superlative shrinking technology.

(SF4) Since the mid-1990s, Japanese chipmakers have started to lose even their comparative advantage in the manufacturing system.



2.1 Confirmation of SF1

SF1 can be directly confirmed by Figure 1, which shows the respective shares of the DRAM

shipment attained by chipmakers in five countries. Indeed we can see that the share of the shipment accounted for by Japanese chipmakers drastically declined from the end of the 1980s onward. During this period, Fujitsu retreated from the business in December 1998, Toshiba in December 2001, and Mitsubishi Electric in October 2002. NEC and Hitachi also spanned off the DRAM business from their main businesses line and jointly established Elpida, a pure-player of commodity DRAM, in December 1999. Currently Elpida is the only commodity DRAM maker remaining in Japan.

2.2 Confirmation of SF2

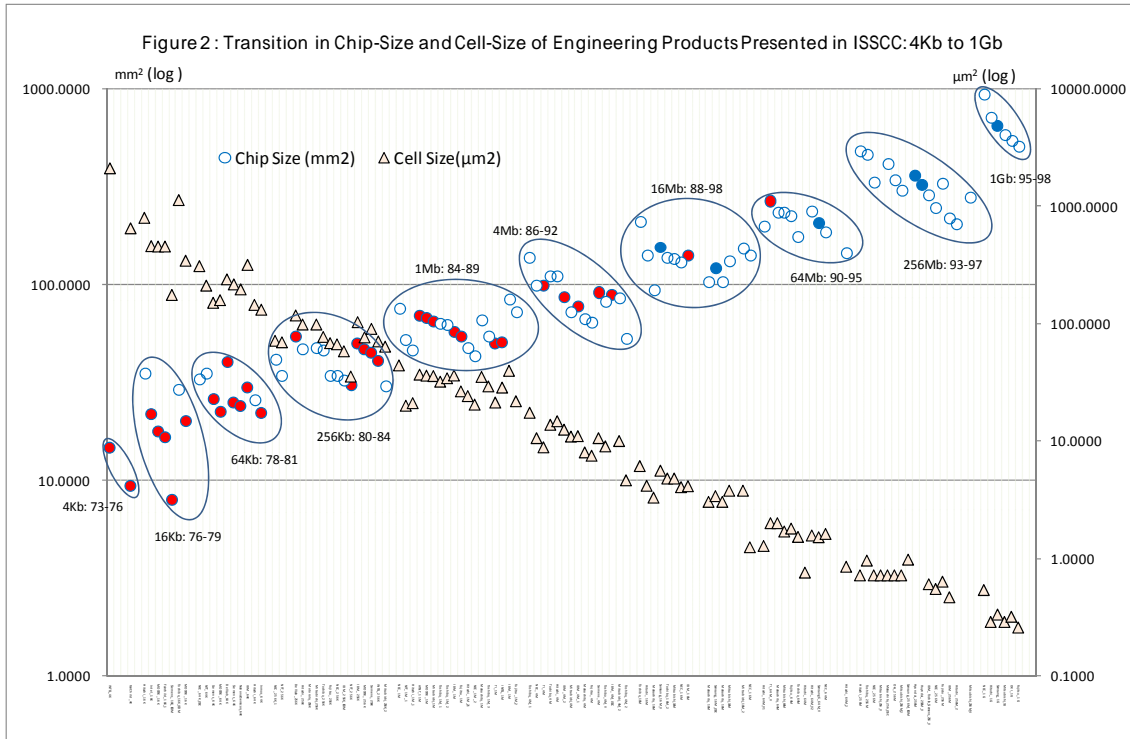
Regarding 256Kb or larger DRAMs, many of core processing and design technologies came from Japan (Hitachi in particular) and the United States (IBM in particular). The situation can be confirmed from Figure 2, where the chip- and cell-sizes¹⁰ of the next-generation DRAMs presented at the International Solid State Circuits Conference (ISSCC) from 1973 to 1998 by various chipmakers are plotted. The right vertical axis of Figure 2 stands for the chip-size and the left one for the cell-size. In addition, each “○” sign stands for the chip-size and the “▲” sign stands for the cell-size. The horizontal axis shows the names of products written with chipmakers’ names.¹¹ Within each generation of DRAM, the names are arranged by their presentation year. The red signs “●” indicate U.S. or European chipmakers, the blue signs “●” Korean chipmakers, and the white signs “○” Japanese makers.¹²

Figure 2 indicates that both the chip-size (○) and the cell-size (▲) have been shrinking with each subsequent generation, following Moore’s Law. The following facts also are confirmed based on this figure: (1) U.S. chipmakers such as INTEL, MOSTEK, TI, and IBM, were dominant until 64Kb. Micron Technology did not make a presentation at all. (2) Japanese chipmakers started to displace these U.S. makers from 64Kb DRAM and were dominant from 256kb to 1Gb. (3) Korean chipmakers (Samsung and Hynix) appeared since 16Mb, but their presence was infrequent, at least until the late 1990s.

¹⁰ Chip-size is the surface area occupied by each chip, normally expressed by square millimeter (mm²). A “cell” is a set of a transistor and a capacitor within each chip. Cell-size is the surface area occupied by each cell, generally expressed by square micron meter (μm²). The transistor is a switching element by which (0-1) information is created. A capacitor is an element to save electric charge temporarily. A huge number of cells are contained within each chip.

¹¹ The names themselves are made unreadable by their tiny font.

¹² One of the 256Mb samples called “Japanese” is actually due to the IBM-Siemens-Toshiba (“Triad”) alliance. The “Triad” started in 1993 (and ended in 1996) to jointly develop 256Mb trench-type DRAMs by using 0.25μm technology together with chemical mechanical planarization (CMP) technology. 64Mb DRAMs by Siemens and Toshiba shown in Table 3 were the results of this alliance.



The above situation is also confirmed (refer to Table 1) by the number of presentations conducted by chipmakers at the ISSCC and the International Electron Devices Meeting (IEDM). The ISSCC is an international conference mainly for semiconductor design technologies, while the IEDM is an international meeting for processing (i.e., fabrication) technologies. Most papers at the ISSCC consisted of only about two pages and took on a strong character of demonstrating chipmakers' leading-edge device-technologies. In contrast, many of the technologies presented at the IEDM preserve a rich flavor of research.

Table 1 indicates that during the 1980s and the 1990s, Japanese chipmakers were actively involved in both design and processing technologies. In each period, IBM also continued to maintain its role as a technological pioneer in both areas. In contrast to Japanese chipmakers and IBM, Micron Technology in the United States did not present papers at ISSCC or did a few at IEDM. The same also applies to Samsung or Hynix until the mid 1990s. In this sense, at least until this period, both Micron and Samsung could be called "chipmakers of a knowledge utilization type." Micron still assumes this position today. In contrast, since the mid 1990s, Samsung has considerably increased its presentations at both the ISSCC and the IEDM.

Table 1: DRAM-related Papers in the ISSCC and IEDM by Chipmakers

1) ISSCC (DRAM-related) * means one paper		1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003
Hitachi	*		*		**	***	**	**	**	**	**	**	**	**	**	**	**	**	**	*	*	*	*	*	*
Toshiba	**		**	*		***	***	*	*	*	*	*	*	*	*	*	**	**	**	**	**	**	**	**	**
NEC	*	*		**	*	*	*	*	*	*	*	*	*	*	*	*	*	**	**	**	**	***			
Mitsubishi Elecatric			*	*	*	*	*	*	*	**	*	*	*	*	*	**	*	*	**	*	*	*	**	*	*
Fujitsu				**	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	**	*	*	*	*
IBM		*	**	*	**	*	*	*	*	**	*	*	*	*	*	*	*	*	*	*	***	*	*	**	*
Intel		*	***	**	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Micron																									
Mostek					*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Motorola				*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Texas Instruments	*						**	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Infineon + Siemens					*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	**	*	*	*
Samsung																		*	**	*	**	*	*	*	*
Hynix + Hyundai + LG																				**	*	*	*	*	*
2) IEDM (DRAM-related)		1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003
Hitachi	*	*	*	*	**	***	**	*	*	*	*	*	*	*	*	*	*	*	*	*	***	***	***	**	**
Toshiba		**		*	**	***	**	*	*	*	****	*	***	*	****	**	**	**	**	***	****	***	***	**	**
NEC	*			*	*	*	*	*	*	*	*	*	*****	****	*	***	****	****	***	****	****	**	**	*	*
Mitsubishi Elecatric	*	*	*	*	*	*	*	*	*	*	*	*	*	*	***	*	****	*	****	*	***	*	*	*	*
Fujitsu								*	*	*	*	*	*	*	*	*	*	*	*	*	**	**	**	*	**
IBM				*	*	*	*	*	*	****	*	*	**	****	*	*	*	*	*	*	*	***	*	****	**
Intel			*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Micron												*	*	*	*	*	*	*	*	*	*	*	*	*	*
Mostek					*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Motorola											*	**	*	*	*	*	*	*	*	*	*	*	*	*	*
Texas Instruments					*	**	**	*	*	*	**	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Infineon + Siemens															*	*	*	*	*	*	***	*	****	***	**
Samsung															*	*****	**	****	*	****	**	***	***	***	***
Hynix + Hyundai + LG																	***	**	*	*	*	*	*	**	**

Sources : IEDM 50 Years (DVD), ISSCC 50 Years (DVD)

2.3 Confirmation of SF3

Despite their unmatched technological advantages with respect to 64 Mb and larger DRAMs, Japanese chipmakers tended to lag behind Samsung for the start of commercializing cutting-edge devices and behind Micron in the speed of shrinking chip-size for tailing-edge devices. The former can be confirmed by Table 2. The first row of Table 2 shows such items as the memory size, the year presented at ISSCC, JSSC, or SVLSIC (A0), the name of the presented chipmakers, the year of the first commercial production (A1), the name of the first chipmaker, etc. According to this table, beyond 64 Mb size of DRAMs, the length of the period from the development to the first commercial production (see (A1-A0)), to a million number of shipments (see (A2-A0)), and to the peak number of shipments (see (A3-A0)) all increased. These facts indirectly exemplify the increased technological complexity in DRAMs beyond 64Mb.

For DRAMs of 64Kb to 16Mb, Japanese chipmakers could have enjoyed the benefits of both pioneers' gains and volume production. Nevertheless, Samsung started to outpace Japanese chipmakers even in the start of commercial production of cutting-edge devices. Indeed, after 128Mb, despite its technological disadvantage relative to Japanese chipmakers, Samsung started to enjoy the benefits of pioneers' gains and mass production benefits as a market leader.

Table 2 : Transition in DRAM Development and Commercial Production by Memory Density

DRAM-Size (Bit)	Presented Year in ISSCC, JSSC, VLASIC (A0)	Presented Makers	Year in First Commercial Production (A1)	First Commercial Production Maker	(A1-A0)	Year when a million number of shipments was attained	(A2-A0)	Peak Year of Number of Shipments (A3)	(A3-A0)
1K	1970	INTEL	1971	INTEL	1	1973	3	1974	4
4K	1972	INTEL	1975	TI	3	1975	3	1979	7
16K	1976	INTEL, Hitachi	1977	Mostek	1	1977	1	1982	6
64K	1978	Mostek, NEC, NTT, Siemens	1980	Hitachi	2	1980	2	1987	9
256K	1980	NEC, NTT	1983	Fujitsu	3	1983	3	1988	8
1M	1984	Hitachi, NEC, NTT	1986	Toshiba	2	1986	2	1991	7
4M	1986	NEC, TI, Toshiba	1989	Hitachi	3	1989	3	1995	9
16M	1988	Hitachi, Matsushita, Toshiba	1991	Hitachi	3	1993	5	1997	9
64M	1991	Hitachi	1994	NEC, Samsung	3	1996	5	2000	9
128M	Nothing	Nothing	1998	Samsung	-	1998	-	2001	-
256M	1993	Hitachi, Matsushita, Mitsubishi, Toshiba	1997	Samsung	4	1999	6	2005	12
512M	Nothing	(IBM:2001)	2003	Samsung	-	2003	-	2008E	-
1G	1995	Hitachi,	2004	Samsung	9	2004	9	2009E	14

Sources : ISSCC, JSSC, SVLSIC, SEMICO(2003), ICE(1997), Nikkei-Shinbun
JSSC=Journal of Solid State Circuits, SVLSIC=Symposium on VLSI

Regarding shrinking technologies, Micron's 16Mb DRAMs overwhelmed the competitors by chip-size and cell-size (refer to Table 3). In this table, both chip-size and the cell-size are indexed as the values relative to those of NEC16M_1 in 1991. DRAMs of each chipmaker are commercial products actually produced in a large volume. NEC shrank the chip size to 71% until 1996, while Micron did to 41% (Micron16M_1) and 28% (Micron16M_2) until 1996 and even to 20% (Micron16M_3) until 1997. This is why competitors could not compete with Micron in the market during 1996 and 1997. The overwhelming presence of Micron at that time was called "Micron shock" in Japan.

Table 3: Trend in Chip Size and Cell Size Shrinking

Product	Expected Year	Chip Size (HEC_16M_1=100)	Cell Size (NEC_16M_1=100)
NEC16M_1	1991	100.00	100.00
Fujitsu16M_1	1992	94.71	113.10
Samsung16M_1	1993	67.55	86.67
Mitsubishi16M_1	1994	69.71	71.43
Hitachi16M_1	1994	65.96	75.30
Hitachi16M_2	1994	67.90	76.19
NEC16M_1	1994	68.64	71.43
Samsung16M_2	1994	63.72	65.48
Hyundai16M_1	1994	86.18	95.24
Fujitsu16M_2	1995	68.11	61.90
NEC16M_2	1996	71.24	74.04
OKI16M_1	1996	73.82	77.38
MoselVitellic16M_1	1996	62.67	65.48
Micron16M_1	1996	40.60	35.48
Micron16M_2	1996	27.51	35.48
ShinNipponSteel_1	1997	69.64	130.95
Micron16M_3	1997	20.06	不明

出典 : Chipworks社、Semiconductor Insights社、<http://smithsonianchips.si.edu/ice/s4.htm>

2.4 Confirmation of SF4

The weakening competitiveness of Japanese chipmakers in manufacturing systems was noticeably evident in the results from a questionnaire survey conducted by UC Berkeley in the 1990s (Leachman and Hoges 1996). According to this survey (see Table 4), regarding cycle time per layer¹³ and on-time delivery, U.S. chipmakers generally outpaced major Japanese chipmakers even in the early 1990s. Interestingly, Japanese chipmakers still excelled in wafer yield (ratio of good dies per wafer) and utilization of microlithography tools. The narrowing efficiency gap between Japanese and U.S. chipmakers during this period could be traced back to the late 1980s. Macher et al. (1998) showed that during the early 1990s, the gap had narrowed considerably for such indicators as probe-testing yield,¹⁴ (direct) labor productivity, and defect density, as well as cycle time.

Table 4: Japan-US Comparison in Fab Performance in the Early 1990s

Metric	Best score	Average score	Worst score	Japan vs. US
Cycle time per layer (days)	1.2	2.6	3.3	-
Line yield per ten layers (%)	98.9	92.8	88.2	++
Murphy defect density - (defects/cm ²)				Overall: ++
0.7 - 0.9 micron CMOS memory	0.28	0.74	1.52	
0.7 - 0.9 micron CMOS logic	0.28	0.79	1.94	
1.0 - 1.25 micron CMOS logic	0.23	0.47	0.96	
1.3 - 1.5 micron CMOS logic	0.21	0.61	1.15	
5X stepper throughput (5X layers completed per machine-day)	724	382	140	+
Direct labor productivity (wafer layers completed/operator-day)	63.0	29.6	8.0	+
Total labor productivity (wafer layers completed/total staff-day)	37.7	17.6	3.3	++
On-time Delivery (% of line items with 95% of die output on time)	100%	89%	76%	-

Average and worst scores are calculated after discarding the worst data sample for each metric. Legend:
 ++ Japanese fabs are almost uniformly superior
 + Japanese fabs are generally superior
 0 Superior/inferior fabs are not distinguished by region
 - US fabs are generally superior
 -- US fabs are almost uniformly superior

Source: Leachman and Hoges (1996)

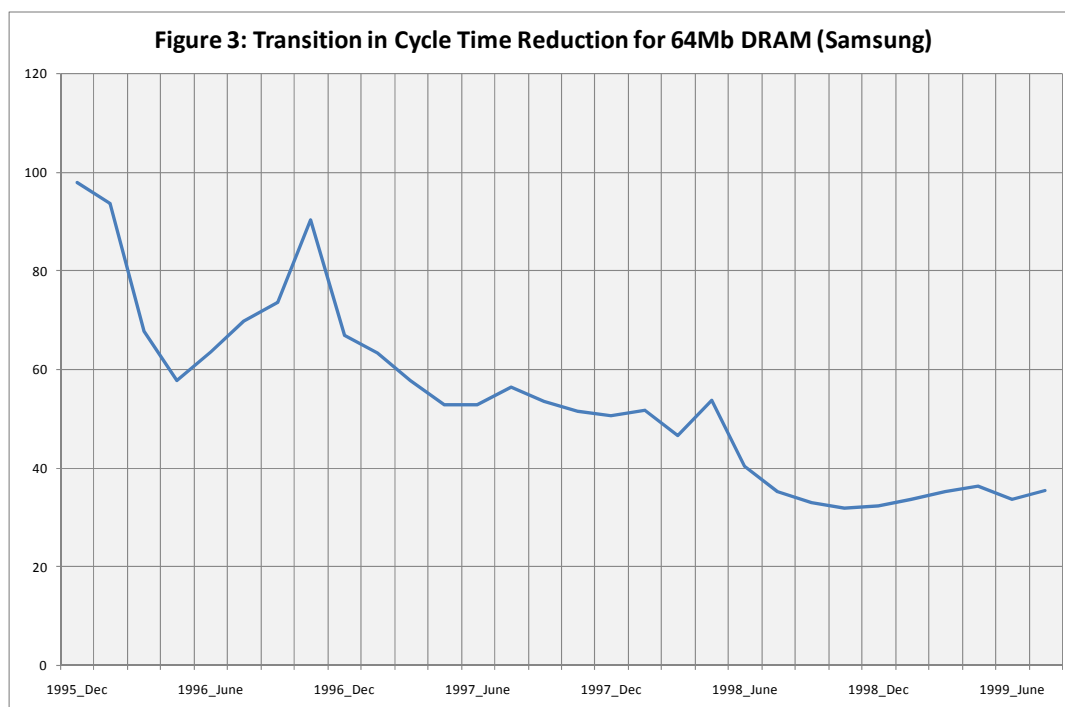
Samsung electronics also had significantly reduced its cycle time in the second half of the 1990s. Indeed, Leachman et al. (2002) fully described the serious attempt at Samsung Electronics to reform the manufacturing system from 1996 onward.¹⁵ As a result of this reform, Samsung's total cycle time (turn-around time: TAT) of 64Mb DRAMs was reduced from 90 days in early 1996 to a little more than 30 days in late 1998 (see Figure 3). In contrast, around 1998, the corresponding TAT of Japanese chipmakers was 60 days or more, on average. The cycle time per layer was also, on average, around 2.0 days among the five leading chipmakers, even in 2001.¹⁶

¹³ Average days needed to process one piece of mask.

¹⁴ "Probe testing" is conducted after completing wafer manufacturing by testers called "probers."

¹⁵ Dr. Leachman was himself worked as Samsung's leading manufacturing consultant.

¹⁶ The date (for logic devices) is based on the field research conducted by one of the current authors.



Source: Leachman et al. (2002)

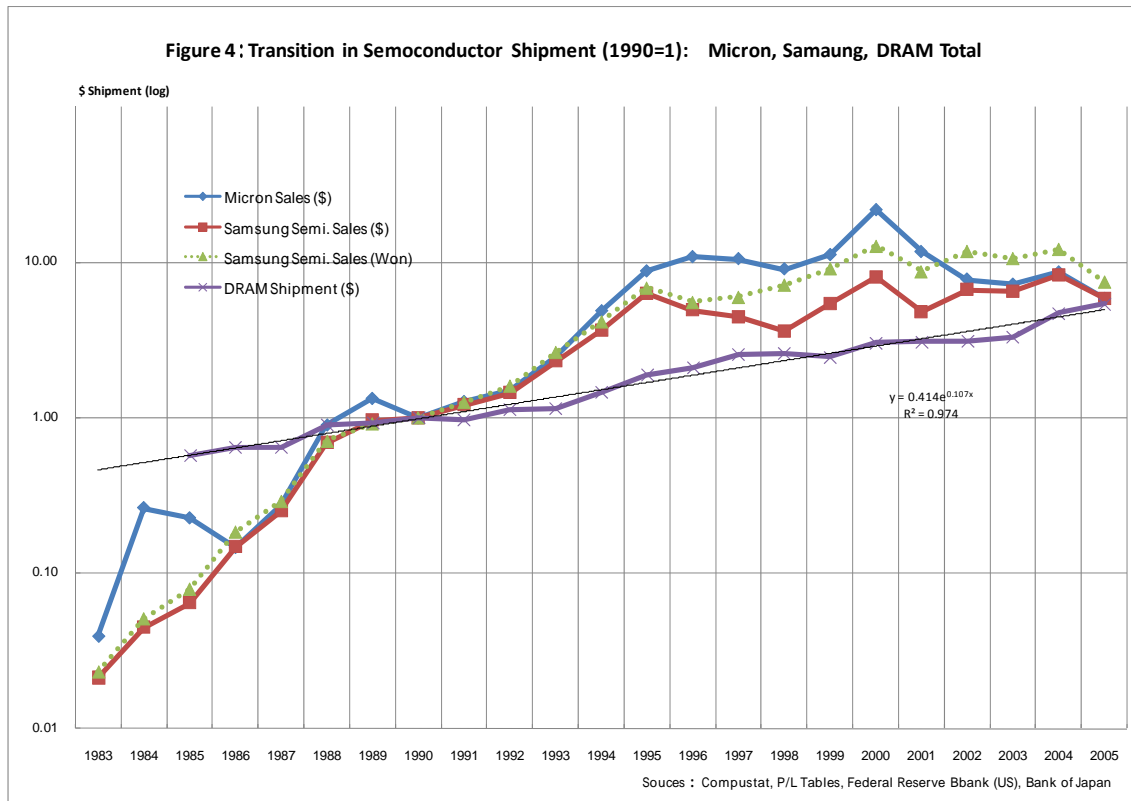
3. The Impact of the Japan-United States Semiconductor Trade Agreement (J_USTA)¹⁷

The pressure on Japanese chipmakers by the U.S. government under the J_USTA was so strong that it went far beyond our imagination today (Ohyane 2002). Indirect as it may be, the impact is shown in Figure 4. The vertical axis of this table is the log-transformed shipment/total sales value (in U.S. dollars) and the values of each series of data are normalized to the 1990 value. Regarding Samsung, the change expressed in won (dotted line) also is shown. In addition, to make a comparison, the change in the value of the world DRAM shipment is indicated, together with the fitted (10% upward-sloping) straight, dotted line.

This figure shows that during the 1986 to 1995 period, both Micron and Samsung achieved quite a high growth rate of 40%. In particular, Micron entered into a slump in 1985, and its sales drastically dropped from 1984 until 1986. Nevertheless, thanks to the J_USTA, from 1987 onward it immediately followed the path of rapid growth. The rapid growth achieved by Micron and Samsung was underpinned by the significant increase in DRAM prices caused by the limited

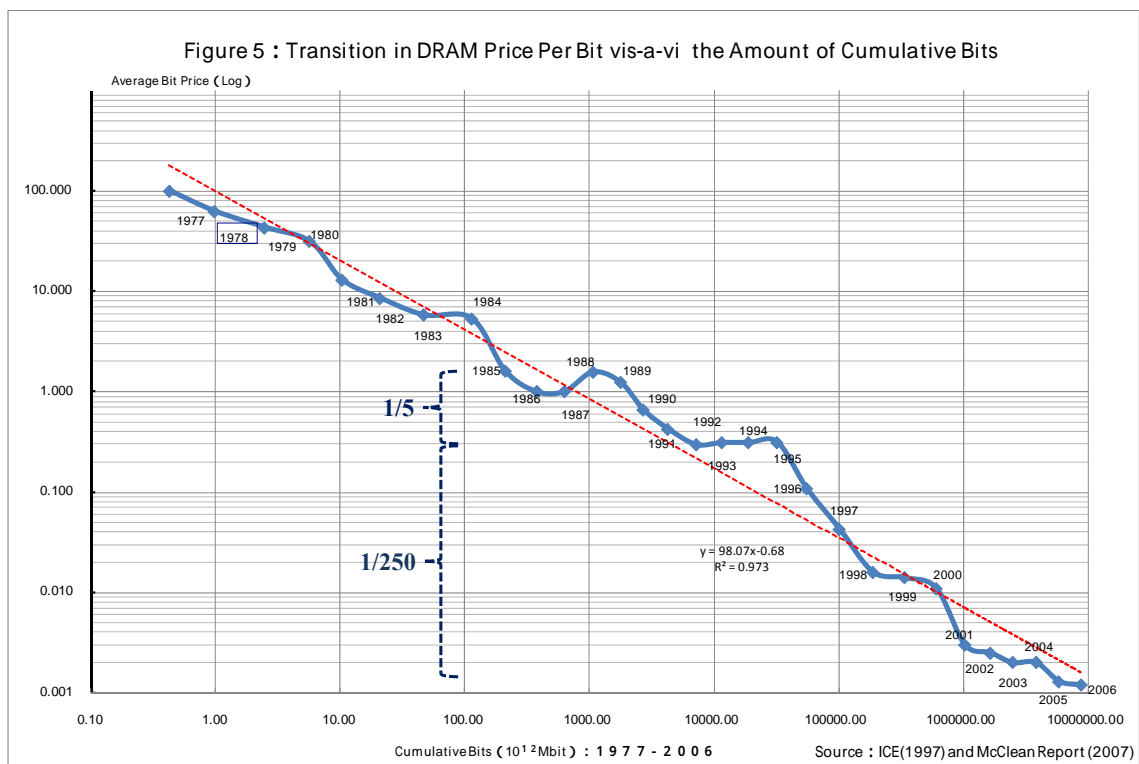
¹⁷ Many people have repeatedly tried to explain some of the four stylized facts (SF1 to SF4) in a fragmentary fashion. They have tended to emphasize, as the principles underlying these facts, the insufficiency and delay in voluminous investment resulting from managerial maldecision, a delayed perception about the structural changes in the (commodity) DRAM market triggered by the advent of PCs, the various severe restrictions imposed on Japanese chipmakers under the J_USTA, and the decline in cost competitiveness because of the drastic yen appreciation relative to U.S. dollars or Korean won. Instead of scrutinizing the relevancy of these hypotheses in detail, because of space limitations, only the decisive impact of the J_USTA will be briefly examined. For a survey of conventional views, see Yoshioka (2004).

supply under the J_USTA. Indeed, according to Johnson et al. (1988), a 4Mb DRAM chip cost approximately four dollars and sold for about twelve dollars in the (spot) market around 1992.



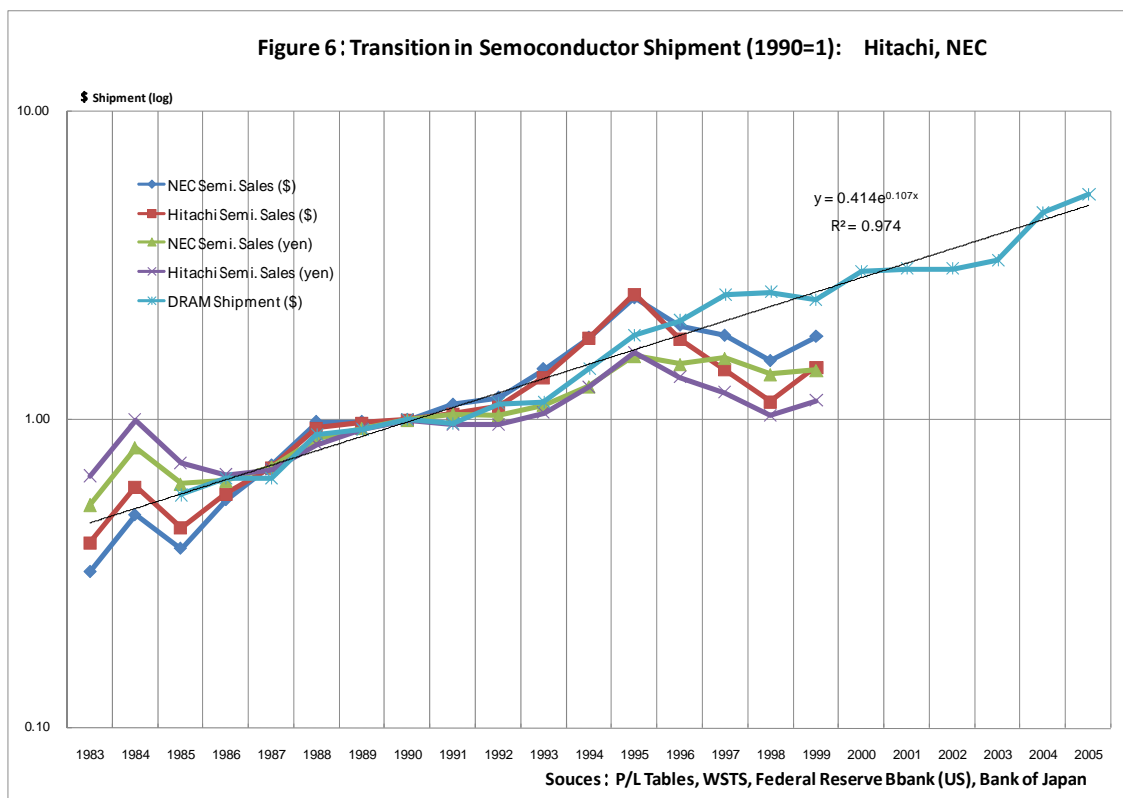
Such an abnormal sellers' market situation can be clearly confirmed through the transition in the average DRAM price per bit, as shown in Figure 5. The vertical axis of this figure stands for the average DRAM price per bit (logarithm) and the horizontal axis for the accumulated bit capacity of DRAMs.¹⁸ Between the annual changes in the DRAM price per bit and the accumulated bit capacity, there is a quite fitted (log linear), downward relationship, with a determination coefficient of 97% (see the straight line in Figure 5). According to this figure, the price per bit significantly rose just after the initiation of the J_USTA, almost constant from 1991 to 1995 and severely dropped from 1996. Actually, the price per bit gradually decreased by 1/5 during the 1985-1995 decade and dramatically dropped by 1/250 during the next decade (1995-2005). Therefore the sudden windfall by the J_USTA provided the strong backdrop for the astounding growth of Micron and Samsung.

¹⁸ The bit capacity for each year is calculated by multiplying the bit capacity and the quantity of production of various sizes of DRAMs produced in each year. The accumulated bit capacity in each year is the amount added up from 1977.



Much smaller as it may be, the windfall effect also spilled over to Japanese chipmakers with restricted capacities. Figure 6 depicts this ironical situation. The vertical and horizontal axes are the same as in Figure 4, but the reduction scale of the vertical axis is twice as small as that of Figure 4, reflecting the low growth rate of Japanese chipmakers. In addition, as the DRAM divisions of Hitachi and NEC merged around late 1999 to form a new DRAM maker, Elpida, no data are available separately after 1999.

Figure 6 shows that during the 1980s to the mid-1990s, Japanese chipmakers grew at almost the same rate of 10% as the world DRAM shipment. So the bubble burst of the Japanese economy in the early 1990s did not have much of an influence until 1995. As shown in Figure 1, Japanese chipmakers' share of the world DRAM market still exceeded that of their South Korean competitors by around 15%. Such a situation, however, drastically changed as a result of the severe decline in DRAM prices starting in 1996. Immediately after 1995, both Hitachi and NEC started to face significant, negative growth (see Figure 6). Although they are not shown in the figure, similar situations were brought about for Toshiba, Fujitsu, Mitsubishi Electric, etc.

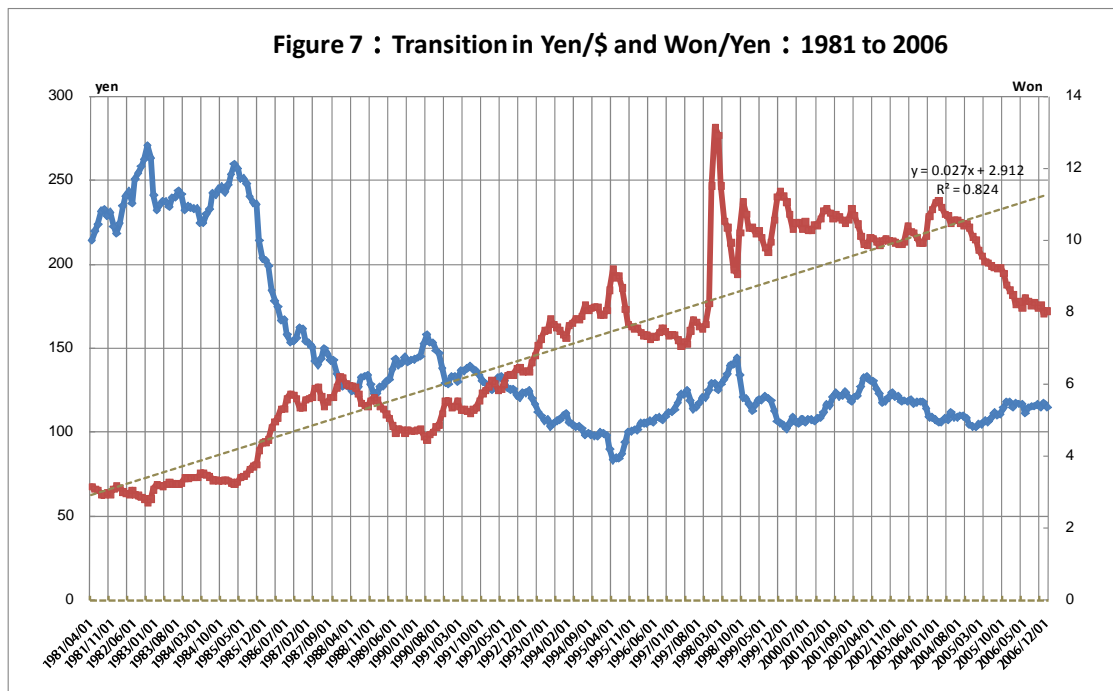


We also note that reflecting the yen depreciation in the early 1980s and the up-and-down appreciation during the decade since the mid-1980s, Hitachi's and NEC's respective growth rates of total sales in dollar values show much larger variability than the ones in yen values. Accordingly, we could not attribute Japanese chipmakers' sudden deceleration from 1995 to the J_USTA and the adverse movement in foreign exchange rates. Indeed, during the period of the second J_USTA from June 1991 until July 1996, the diplomatic pressure from the United States was lightened somewhat (Ohyane 2002, pp.217-220). However, under the J_USTA, partly due to strong guidance from the Japanese government, most major Japanese chipmakers, except for Toshiba, directly invested in self-owned overseas fabs, which might be regarded as quite reckless if judged by today's criteria. Those fabs had been inevitably closed or retreated without exception.¹⁹ This might have considerably deprived Japanese chipmakers of their freedom to domestically invest in cutting-edge wafer fabs.

In addition, it is necessary to note the trend in the yen/dollar and won/yen exchange rates as one of the crucial factors advancing Samsung's great progress in the latter half of the 1990s (see Figure 7). The appreciation in yen (/dollar) quickly showed up in the mid-1980s and strengthened its tendency until 1995, which might have been a headwind for Japanese chipmakers and a fair

¹⁹ Certain chipmakers have signed a binding agreement with foreign governments to maintain their fabs.

wind for Micron. Since the late-1990s, however, the yen/dollar exchange rates have been relatively stable. Won/yen exchange rates continued to depreciate about 0.3 won per yen each year for about 25 years, which gave Samsung huge long-term benefits. Hence, together with the collapse of DRAM prices at the 1995 year-end, such marked won/yen depreciation created a difficult situation for Japanese chipmakers.



4. Cause and Effect of the Stylized Facts: Endogenous View

In this section, we investigate the cause-and-effect process through which the aforementioned stylized facts (SF1)-(SF4) came into being. To do that, we pay particular attention to the considerable changes in commodity DRAM markets that have occurred since 1996 and the increasing complexity in process technologies urgently required for the commercialization of 64Mb DRAM.

4.1 Loss of Pioneers' Gains and Mass Production Benefits: Between Scylla and Charybdis

Around the mid-1990s, Japanese chipmakers started to lose mass production benefits as well as pioneers' gains on cutting-edge DRAM. Such a situation is reflected in Figure 8, which shows the transition in the chip size of various DRAM generations and the corresponding price per chip area. The vertical axis on the left side of this figure stands for the chip size (logarithm value) and

the one on the right side for the corresponding price per square millimeter.²⁰ On the horizontal axis, a total of 145 mass-produced DRAMs are arranged according to DRAM generation (1Mb to 512Mb). Within each generation, the chips are arranged from the left to the right according to the manufacturing year. The “▲” signs in the figure stand for the chip-size of each mass-produced DRAM, while all colors of “○” signs do the same for their prices²¹ per square millimeter. For example, within an elliptical circle specified as “64Mb” in Figure 8, the mass-produced 64Mb DRAMs of various chipmakers are arranged from the left to the right according to the manufacturing year (the so-called “date code” printed on the chip²²).

Within each generation circle, both the chip-size and the chip-price per area tend to become smaller over the years. There are also few signs of ○ in the upper region, but many such signs in the lower region. The higher a ○ sign goes, the more expensive the chip-price per area is, so that pioneers in cutting-edge DRAM could have first-mover gains. Within Figure 8, the red signs “●” stand for Samsung’s chips, the blue ones “●” for Micron’s, and most of white ones “○” for Japanese chipmakers’.

According to this figure, Japanese chipmakers enjoyed both pioneers’ gains and mass production benefits until 4Mb, Samsung started to have mass production benefits from 64Mb and pioneers’ gains, in addition, from 128Mb, and Micron started to have mass production benefits from 16Mb. In addition, based on Figure 8 and the utilized data, the following facts are observed.

- 1) For 1Mb or 4Mb, Japanese chipmakers enjoyed both pioneers’ gains (Toshiba, Hitachi, Fujitsu) and mass production benefits (Hitachi, NEC, Toshiba, Fujitsu, Mitsubishi).
- 2) For 16Mb, NEC and next Fujitsu had pioneers’ gains in 1991 or 1992, and Samsung and Japanese chipmakers (Mitsubishi, Hitachi, and NEC) had mass production benefits around 1993 or 1994 and Micron during 1996 to 1997.
- 3) For 64Mb, Hitachi had a pioneer’s gain in 1993 and Siemens (together with IBM) and Samsung also both did so in 1995, mainly because that was the year just before the collapse of commodity DRAM prices.²³
- 4) For 128Mb, Samsung had a pioneer’s gain in 1998 and Japanese chipmakers (NEC, Toshiba) tried in vain to have mass production benefits in 1999.
- 5) For 256Mb, Samsung had a pioneer’s gain in 1998, and both Samsung and Micron had

²⁰ Both chip-size and cell-size data mainly come from the analysis reports by Chipworks Inc. (<http://www.chipworks.com/>), *Semiconductor Insights* (<http://www.semiconductor.com/>), the Smithsonian’s “ICE Collection” (<http://smithsonianchips.si.edu/ice/icesum.htm>), and the *EETimes* (<http://www.eetimes.com/>), the article by Dev Paul, 06/10/2004). A few data also were found in the *Nikkei Newspaper*, *Nikkei Microdevice*, etc.

²¹ Refer to SEMICO Research (2003) for the price.

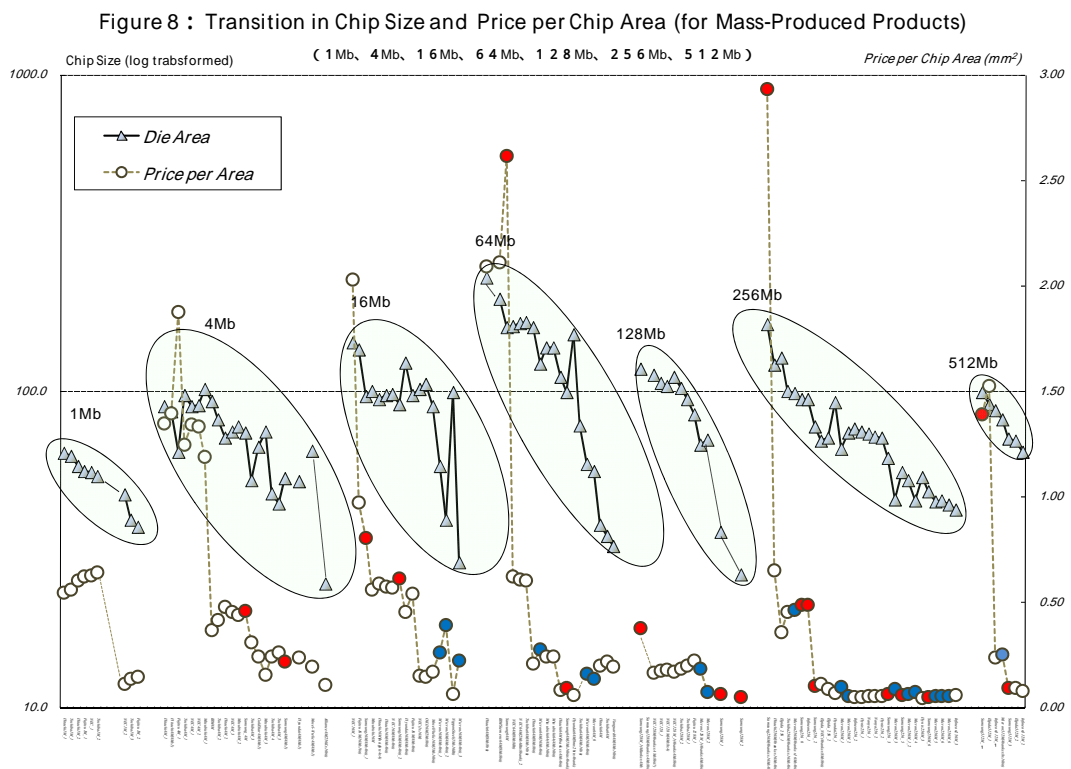
²² To finally determine manufacturing years, we thoroughly checked several representative websites of various DRAM resellers in the world, as well as the date codes indicated in the purchased analysis reports.

²³ Hitachi’s and Siemens’s chip-prices were significantly lower than Samsung’s because Hitachi’s and Siemens’ chip-sizes (229 mm² and 197 mm², respectively) were quite larger than Samsung’s (159 mm²).

mass production benefits, although Micron enjoyed a slight advantage in the chip-shrinking competition.

6) For 512Mb, Samsung had a pioneer's gain in 2003.²⁴

These facts clearly indicate that many Japanese chipmakers were driven to the wall, between Scylla (Samsung) and Charybdis (Micron), in the commodity DRAM market of 64 Mb or larger.



4.2 Root Causes of Losing Pioneers' Gains: Tardy Technology Marketing Strategy?

Figure 8 displays one more noteworthy tendency: that the commercial DRAM capacity had quadrupled until 64Mb in a manner like 1Mb→4Mb→16Mb→64Mb, whereas beyond 64Mb, the capacity has come to be duplicated in a manner like 64 Mb→128 Mb→256 Mb→512 Mb. This newly observed phenomenon reflects not only the increasing complexity of manufacturing advanced DRAMs, but also the rapid structural change in the semiconductor market after the collapse of commodity DRAM prices. Actually, most Japanese chipmakers could not effectively cope with this unexpected change. One crucial reason was the stalling speed of the synchronization among the research, development, manufacturing, and marketing/sales divisions within each

²⁴ For 512Mb, the available data are very limited.

corporation.

In contrast, until 1993, when commercial production began in the state-of-the-art 200mm fab, Samsung already had completed its transformation from the linear R&D system, in which the R&D division is clearly separated from the manufacturing division, to the chain-linked R&D system in which activities in these divisions are concurrently synchronized. The highlight was the Process Architecture (PA) system that tried to concurrently overlap the tasks of R&D engineers (belonging to the PA section) and those of process/equipment engineers responsible for mass production.

Furthermore, Samsung started to implement a new marketing strategy called “Strategy for Increasing the Accuracy of Marketing Information” in 1994. Before implementing this strategy, the group of application engineers who exclusively belonged to the corporate sales division outside the memory division was responsible for making marketing strategies based on the sales data that were collected from specific customers in a face-to-face manner. In contrast, under the new strategy, the cross-functional “Product Planning Team” was required to make and implement a comprehensive marketing strategy by utilizing short- and long-run information. Around the mid-1990s, Samsung was still behind, relative to Japanese competitors, in advanced element process technologies so that the above two reforms certainly hit the mark.²⁵

As a result, Samsung could have had a pioneer’s gain for 128Mb in 1998, and all of Japanese chipmakers except for Hitachi tried to have mass production benefits of 128Mb in 1999. However, the resulting oversupply unintentionally provoked the price freefall of 128Mb right before the collapse in 1996. In fact, the 128Mb DRAM price dropped to half in a year, a third in two years, and one-twenty fifth (7%) in three years. Then eventually all Japanese chipmakers retreated from the market one after another: Fujitsu in 1998, Hitachi-NEC joint venture (Elpida) in 1999, Toshiba in 2001, and Mitsubishi in 2002. Hitachi did not even commercialize 128Mb at all and instead tried to introduce the specific 128Mb memory module by using its ultra-small 64Mb chips in 1999. But it could not catch up with drastically falling prices to retain profits.

In addition, Samsung managed to start selling both 128Mb and 256Mb DRAMs in the same year of 1998.²⁶ Their chip- and cell-sizes were also small enough to be accepted in the market: 128Mb DRAM (chip size: 118mm^2 , cell-size: $0.52\mu\text{m}^2$) and 256Mb DRAM (chip size: 164mm^2 , cell-size: $0.36\mu\text{m}^2$). Indeed, as is displayed by two large arrows in Figure 8, until 64Mb DRAM, the chip size tended to be larger than before generation after generation. Such a tendency, however, discontinuously vanished from 128Mb DRAM so that nearly no chips with a size larger than 100mm^2 could exist as a mass-produced product any longer.²⁷ Consequently, seizing the brief moment

²⁵ Samsung’s reforms are described in Chou (2007).

²⁶ In the 8th week of 1998, Samsung commercialized “Model KM48S16030T-GL” for 128Mb and in the 48th week of 1998, “Model KM44S64230AT-GL” for 256Mb.

²⁷ Since the mid-1990s, the chip-size of Micro Processor Units (MPUs) manufactured by INTEL and AMD has been also constant (see Skinner (2007): McClean Report 2007, Figure 14-2 in Chapter 14).

when Japanese competitors were pausing for a breath to determine their directivity, Samsung jumped into the market in full force to sweep them aside.

4.3 Root Causes of Losing Mass Production Benefits: The Weakened Wafer Manufacturing System²⁸

Since the collapse of commodity DRAM prices in 1996, mainly resulting from worldwide, sporadic overcapacities, they have been recurrently plunging in one-half or one-third in a short period. Consequently, to cope with enormously increasing opportunity (time) costs, cycle-time reduction with small work-in-process (WIP) became a vital factor in successfully competing for market advantage.²⁹ However, when the cycle time reduction became important, Japanese chipmakers started to irrevocably lose their competitiveness, particularly in 200mm fabs.³⁰

One crucial factor was the advent of “Open MES”³¹ in the early 1990s developed by Texas Instruments (TI) together with the SEMATECH³² as a result of the (national) Microelectronics Manufacturing Science and Technology (MMST)³³ Program (1987 to 1993). To radically reduce cycle time and unravel increasing manufacturing complexity, the Open MES adopted the architecture of a “Lean Manufacturing system (LPS)” *a la* Toyota. Indeed the top-ranking development leader of TI’s Open MES notably mentioned: “Today’s manufacturing demands fully integrated dynamic systems which directly support the concepts of lean, flexible and agile manufacturing to high quality standards” (McGehee et al. 1994).

The necessity of Open MES is also plainly articulated by Alan Moser,³⁴ one of the key architects of the IBM Open MES called “SuperPoseidon” (now “SiView”): “Traditionally, these MES solutions have been home-grown spaghetti-code monsters that have so evolved over time to be nearly unmaintainable.” “The 1970s technology and code behind these systems can no longer keep up with the technical vitality of the industry and therefore, new solutions are needed.” Accordingly, it stands to reason that the LPS *a la* Toyota was immediately exported, from the United States, to European, Korean, and Taiwanese chipmakers.³⁵

²⁸ The root causes of weakening Japanese wafer manufacturing systems are thoroughly discussed in Chuma (2007).

²⁹ Hopp and Spearman (2000:490) emphasized the following five benefits for reducing cycle time and WIP: ***better responsiveness to the customer, maintaining flexibility, improving quality, relying less on forecasts, and making better forecasts.***

³⁰ The era of 200mm fabs started in the early 1990s.

³¹ MES stands for Manufacturing Execution System. “Open” means here that the interfaces among various semiconductor tools are made publicly standardized and compatible. To accomplish such openness, CORBA (Common Object Request Broker Architecture) played a very important role, “which enables and regulates interoperability between objects and applications across heterogeneous languages and computer boundaries” (Lin and Jeng 2006).

³² A consortium of U.S. semi-conductor manufacturers.

³³ For details, see Beave et al (1994), Sullivan et al. (1994), and United States Congress (1993).

³⁴ <http://www.omg.org/docs/telecom/98-03-11.pdf>

³⁵ For example, Siemens introduced the “Workstream” by Consilium (now Applied Materials) into its 200mm fab at Dresden in 1995, Samsung did the “Factory Works” by Fastech Inc. (now “300 Works” by Brooks Automation Inc.) in its 200mm Fab at Kiheung in 1995, and TSMC did the “Promis” by Promis, Inc. (now by Brooks Automation

The Open MES and LPS must be a lock-and-key concept in the age of speed-to-market. Japanese chipmakers, however, stuck to their own developed MES until the late 1990s (Uruga 1997) and the outdated manufacturing system called a “push system”³⁶ (*vis-a-vis* “(market) pull system” *a la* Toyota) around 2000.³⁷ Once opportunity costs turned out to be crucial, it became clear that push systems are appropriate for neither commodity DRAMs nor logic devices. For example, Leachman and Ding (2007) try to calculate the huge total benefits of cycle time reduction in 64Mb-DRAM, exemplified in Figure 3, at Samsung during the 1996 to 1999 period. Despite this fact, why had many Japanese chipmakers floundered into push systems?

One crucial reason must be closely related to the long-established cost management system, the so-called “standard full-costing system,”³⁸ the blind use of which was severely criticized in the late-1980s by Johnson and Kaplan (1988) as the “Relevance Lost.” Actually, around 2000, the relevance lost phenomena could be found almost everywhere in various Japanese industries. This must be one of compelling reasons why, regardless of manufacturing or non-manufacturing industries, quite a few Japanese companies started introducing Toyota-like systems to reduce cycle time and inventories around 2000 with so-called Toyota consultants’ assistance.³⁹ In this sense, the semiconductor industry is not an isolated exception.

The pervasiveness of push systems among Japanese chipmakers in the 1990s could be indirectly confirmed by a comparison of inventory turnover periods (ITP) between U.S. and Japanese chipmakers in Figure 9.⁴⁰ Based on balance sheets and profit and loss tables, ITP is defined as “inventories over costs of goods sold.” A high ITP means the inefficiency of production and/or distribution systems because of a large WIP (work in process) or product inventories. According to Figure 9, U.S. chipmakers, particularly IBM, had started to greatly reduce ITP in a crisis since 1989 when “Cash Flow Statements” became imperative duties for public firms in the

Inc.) in its first 200mm fab at Hinschu in 1996.

³⁶ Hopp and Spearman (2000:340) neatly characterize the “push system” and “pull system” as follows. “A push system schedules the release of work based on demand, while a pull system authorizes the release of work based on system status.” “Briefly, pull systems are **More efficient**, in that they can attain the same throughput as a push system with less average WIP, **Easier to control**, since they rely on setting (easily observable) WIP levels, rather than release rates as do push systems, **More robust**, since the performance of a pull system is degraded much less by an error in WIP level than is a push system by a comparable percentage of error in release rate, and **More supportive of improving quality**, since low WIP levels in pull systems both require high quality (to prevent disruptions) and facilitate it (by shortening queues and quickening detection of defects)” (p. 430).

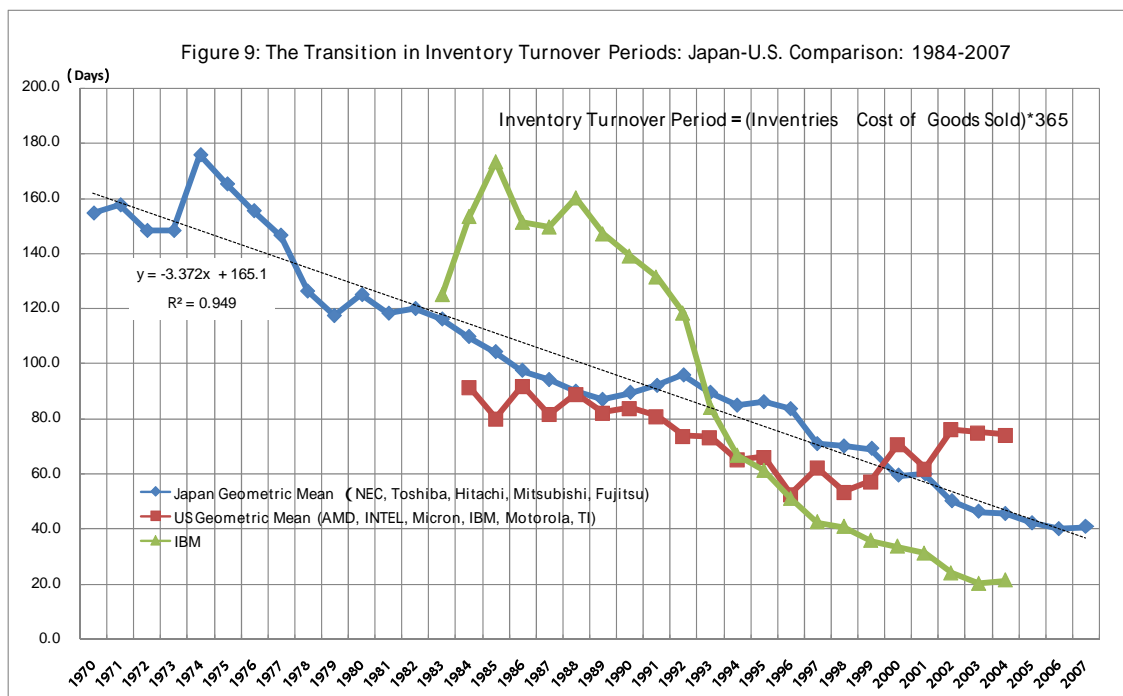
³⁷ There has been a persistent, commonsense view among Japanese semiconductor fabrication engineers: The push system is suitable for low mix and high volume (LMHV) devices like DRAM, while the pull system is suitable for high mix and low volume (HMLV) devices such as SOC (System on a Chip).

³⁸ In standard, full-costing systems, indirect (fixed) costs generally are allocated to each product based on operating hours of machines, equipment, or direct workers. Product inventories or WIP are also treated as assets, irrespective of carrying added or non-added values.

³⁹ For example, based on field research about three representative refrigerator makers in Japan, Chuma (2005) reported that until around 2000, these three companies tended to keep a huge amount of WIP and product inventories within their push systems. Their production lead time was 40 to 60 days around 2000 and it became only 6 days. Of course, quite profitable Japanese companies like Toyota, Kyocera, Rohm, Kao, etc. have not followed suit (e.g., Kawada (2004) or Hiki (2006)).

⁴⁰ The data are based on single statements. The consolidate statements are available only from 1984. The tendency in both sets of data is almost the same.

United States.⁴¹



In contrast, Japanese chipmakers did not reduce ITP at all, particularly during the period of 1989 to 1995.⁴² As was mentioned before, during this period, a sellers' market was extremely prevalent for commodity DRAMs because of the supply constraints imposed by the Japan-United States Semiconductor Trade Agreement. Only after the collapse of commodity DRAM, the ITP of Japanese chipmakers tended to turn back to the historical trend line in the figure. This tendency has become especially prominent since 1999 (March, 2000 in the figure) exactly when the "Cash Flow Statements" became imperative duties for public firms in Japan, a decade behind those in the United States.⁴³

⁴¹ It should be also noted that the Open MES has been introduced together with the activity-based costing (ABC) management software jointly developed by SEMATECH and WWK (Wright Williams & Kelly) since 1991. ICE (1997) described the situation at the U.S. chipmakers around 1990 as "Many companies use activity-based costing (ABC) to determine the relationship between the cost of devices produced by a fab and each of the components that contribute to this cost. Typically, ABC is implemented by forming the ABC team, developing the ABC model, costing the product line, planning cost reduction efforts, implementing cost reduction, and evaluating results. Cross-functional teams typically contain employees from all factory departments including finance, purchasing, technology development, process engineering, equipment engineering, production control, and facility groups. The ABC model demonstrates cost per wafer sensitivity to composite yield, production volume, utilization rate of existing equipment, and the cost of purchasing new equipment." The implementation example at AMD reported in Cooper et al. (1993) is also very interesting.

⁴² Note that "1996" in the figure means "March 1996" for Japanese chipmakers because of the definition of their financial years. The same rule is also applied to the other years.

⁴³ We also note here that the "Relevance Lost" phenomena are still quite likely to happen in Japanese chipmakers mainly because their semiconductor divisions were just a part of large, vertically integrated companies (so-called Integrated Device Manufacturers (IDM)). In particular, the extraordinarily powerful system divisions in these IDM

The sophisticated automatization of wafer manufacturing systems necessitated by Moore's law also started to bring about one more bewildering change in the division of labor among operators/technicians and engineers within many Japanese fabs. Indeed, to effectively cope with the enormous extension of interdependence among fabrication processes, most Japanese chipmakers tried to transform, with the advent of highly automated 200mm fabs, their conventional "autonomic (manufacturing) systems," where self-governing skilled operators/technicians play critical roles as complementary problem-solvers, into "automatic systems," where they are mostly substituted by automatic systems *per se* or engineers. The above push systems that intrinsically pursue local optimization (Hopp and Spearman 2000) further spurred this tendency.

Ironically, however, highly automatized systems develop a high propensity for creating the notable interferences between manufacturing systems and people's motivations or sense of self-fulfillment. This is mainly because they could greatly enhance people's higher-order intelligence for problem-solving or rule-discovering, as well as capabilities for calculation and memory (Nishida 2005). Then, even people's simple negligence or minor human errors unexpectedly are apt to upset WIP balances or constant wafer movements on an enormous scale through all of the fabrication processes.⁴⁴

Therefore, if it is effectively implementable, autonomic systems *a la* Toyota could behave more tactfully than automatic ones *a fortiori* for the highly complex processes or products. From the beginning, as is repeatedly confirmed in various studies (e.g., Koike et al. (2001), Japanese manufacturers tend to have a clear comparative advantage in implementing these autonomic systems. Although most of them have again successfully transformed, in particular since around 2000, the previous automatic systems into the autonomic ones exemplified by Elpida (see Chuma 2007), Japanese chipmakers characterized by automatic systems rapidly lost their competitiveness in wafer manufacturing in the 1990s.

4.3 Root Causes of Failing to Exploit Their Own Technological Advantages

Even though DRAM makers could stand out in marketing and manufacturing technologies, it must be quite difficult to obtain pioneers' gains or mass production benefits (especially through chip-shrinking) without having sufficient science-knowledge integration or utilization capabilities. If so, how could Samsung or Micron outweigh their apparent technological disadvantages? To

tend to behave like fabless makers to look upon their semiconductor divisions as one of favorite foundries. Although the ratio of indirect costs have been enormously increasing at an alarming rate at their semiconductor divisions, those costs must be, in effect, mostly variable ones for them, so that IDM as a whole has no direct incentive to carefully allocate immense indirect costs accruing from the semiconductor division by adopting cumbersome ABC-type full costing management systems.

⁴⁴ Indeed, in such exceedingly interdependent systems, the following *organization principle* comes in: "When a system evolves to become more complex, this always involves a compromise: if its parts become too separate, then the system's abilities will be limited---but, if there are too many interconnections, then each change in one part will disrupt many others" (Minsky 2006:104).

answer this fundamental question, we have to pay special attention to key process technologies first widely applied to 64Mb DRAMs.

A. Three Key Process Technologies

In commercializing 64Mb DRAMs, three important technologies have been newly and intensively utilized: (a) three dimensional (3D) capacitors⁴⁵ called “stack-type (stacked)” or “trench-type (trenched),” (b) hemispherical grains (HSG), and (c) chemical mechanical planarization (CMP). 3D capacitor is a process technology to widen the surface area of conductors and insulators. It could make the capacitance of each miniaturized cell (a pair of transistor and capacitor) much larger than a planar capacitor. Invented as both of them were by Hitachi in the early 1970s, stack-type DRAMs were first commercially used for 4Mb (commodity) DRAMs by Fujitsu and then Hitachi, NEC, Samsung, Micron, etc. and trench-type DRAMs by IBM, Toshiba, Siemens, and TI in the late-1980s.

HSG is a process technology for stack-type DRAMs to increase the storable charge in capacitors several times larger than otherwise by making the surface of the (bottom polysilicon) conductor rugged or textured.⁴⁶ As is shown in Table 5, when NEC originally invented HSG in the late-1980s, it was first commercially applied to 64Mb DRAM by Micron in 1997 and then by NEC and Samsung almost simultaneously in 1998.

Table 5 : The Introduction of HSG or CMP Process Technology for 64Mb Commodity DRAMs

Key Process Technology	1995	1996	1997		1998	1999
Stacked Capacitor with HSG			Textured polysilicon with CUB	Textured polysilicon with COB	Textured polysilicon with COB	Textured polysilicon with COB
			Micron	Mitsubishi	Samsung, NEC	Hitachi
CMP	For Interconnect & Transistor	For Interconnect & Transistor	Only For Interconnect		For Interconnect & Transistor	For Interconnect & Transistor
	SIEMENS	Toshiba	Micron		Micron	Hitachi

Sources : Chipworks, Semiconductor Insights, <http://smithsonianchips.si.edu/ice/s4.htm>, Tatsumi et. al. (2002) and Interviews

Note 1) COB=Capacitor Over Bit Line, CUB=Capacitor Under Bit Line

⁴⁵ A capacitor is structured to place an insulation (thin dielectric) film between two conductor plates (polysilicon layers). *Ceteris paribus*, the larger the surface area of a conductor is, the large electric charge it can save.

⁴⁶ HSG is not compatible with trench capacitors because of its limited ability to withstand high-temperature processing (El-Kareh (1997), http://sst.pennnet.com/Articles/Article_Display.cfm?Article_ID=5462&pc=gl). The capacitor structure made by HSG is called "textured," "texturing," "rugged," and "modulated stacked" (Tung, Sheng, and Yuan 2003).

CMP is a revolutionary process invented by IBM in the early 1980s that can remove topography from silicon dioxide, poly silicon, or metal surfaces with a hybrid of chemical etching and free abrasive polishing.⁴⁷ IBM granted this CMP technology to Intel in 1987 and to Micron in 1988 (Perry 1998). Conventional planarization technologies, such as Spin-on Glass (SOG) and Resist-Etch-Back (REB), required great dexterity in applications, which became avoidable by CMP. Moreover, if the ideal flatness was achieved by CMP, latitude in designing and manufacturing was dramatically enhanced (Sunami 2006) and chip yields could be boosted.⁴⁸

As far as 64Mb stack-type DRAMs are concerned, CMP was first commercially applied by Micron to 64Mb DRAM in 1997 at interconnect and transistor⁴⁹ layers in 1998 (see Table 5). Except for Toshiba's trench-type DRAMs, Japanese chipmakers specialized in stack-type DRAMs quite late to introduce the CMP process. Indeed, Hitachi first commercially applied CMP to interconnect and transistor layers in 1999.⁵⁰ Korean chipmakers such as Samsung were also very late in commercially applying CMP to both interconnect and transistor layers

B. How Could Samsung Obtain Pioneers' Gains?

As was mentioned above (also see Table 5), when NEC invented HSG in the late-1980s, Samsung was able to commercially apply HSG to its 64Mb DRAM in the same year (1998) as NEC did. Moreover, Samsung could get pioneers' gains by first commercializing its 128Mb DRAM. To aggressively pursue this process, in 1995 Samsung initially introduced a relatively large chip-size of 64Mb DRAM (chip-size=159.3 mm², cell-size=1.2μm²) and then applied HSG to this 64Mb device in 1998 to get its shrunk version (chip-size=100.0 mm², cell-size=0.9μm²).⁵¹ The HSG applied to Samsung's second device in 1998 might have come from NEC, mainly because NEC and Samsung agreed to jointly develop the specific cell for 256Mb DRAM in 1994 and the corresponding fabrication technology in 1996.⁵² This process can be concretely displayed with the corresponding pictures in Figure 10. Consequently, to promptly respond to the strong demand for a much larger capacity of DRAM by suppliers of low-end PC servers or workstations, Samsung commercialized 128Mb DRAM in early 1998.

⁴⁷ IBM first applied CMP technology to interconnect layers of its mass-produced 4Mb DRAM in the late 1980s (http://www-03.ibm.com/ibm/history/history/year_1989.html). For details, see Perry (1998) and Fury (1997).

⁴⁸ This fact is based on the hearing from the technologist of ex-Toshiba in 2007. He said that *ceteris paribus*, chip yields increased from 40% to 70% or 80%.

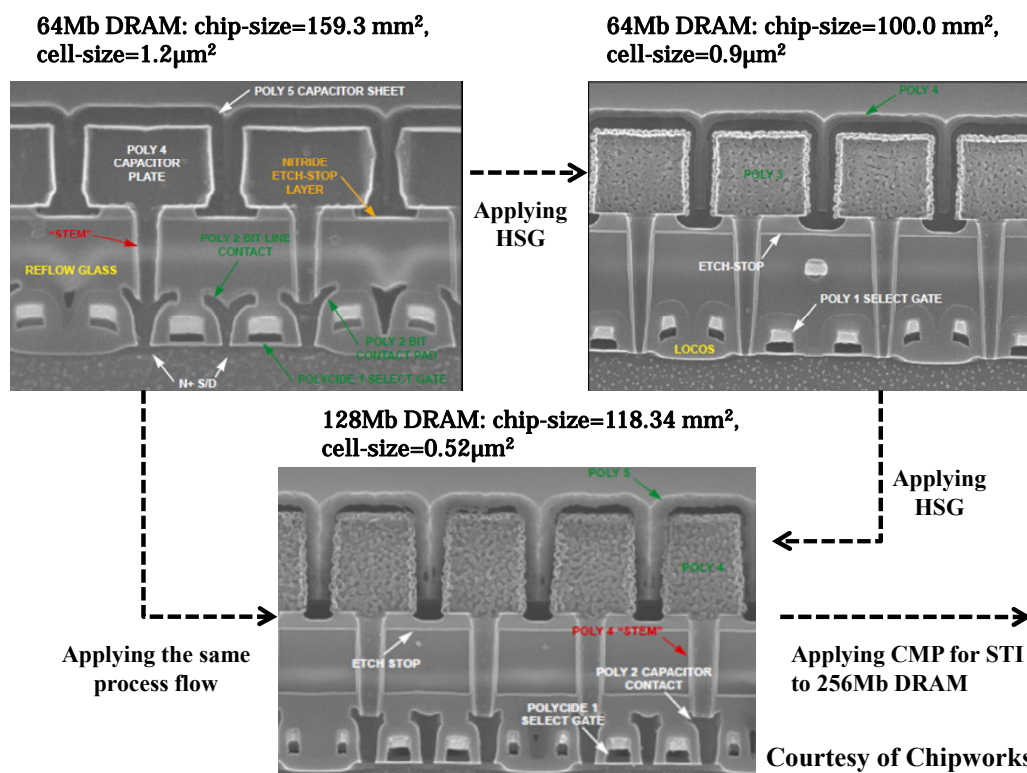
⁴⁹ Precisely speaking, it was first applied to attain shallow trench isolation (STI) that provides a planar surface for further processing. For details, see Wolf (2004:68).

⁵⁰ It is generally said that applying CMP was much easier for trench-type DRAMs than stack-type ones.

⁵¹ The corresponding names of the products are, respectively, KM48V8100AS-6 and KM416S4030BT-GH.

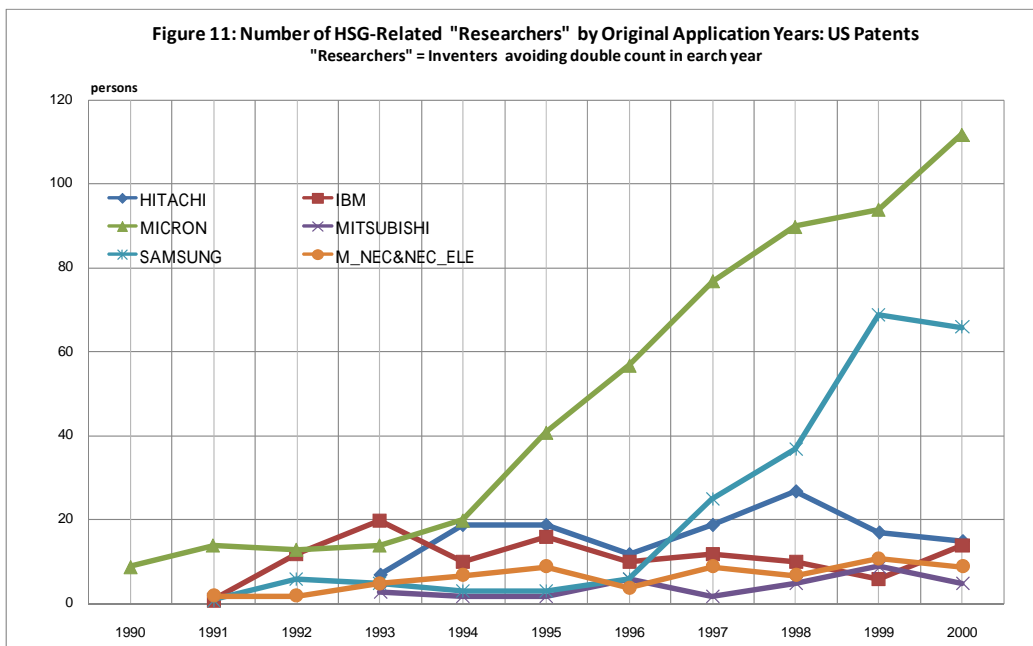
⁵² The mutual exchange of R&D engineers was implemented almost once a month (*Nikkei Keizai Shimbun* dated March 20, 1996 and Mathews and Cho 1999:137).

Figure 10: Samsung's Process of Introducing HSG for 64Mb and 128Mb DRAM

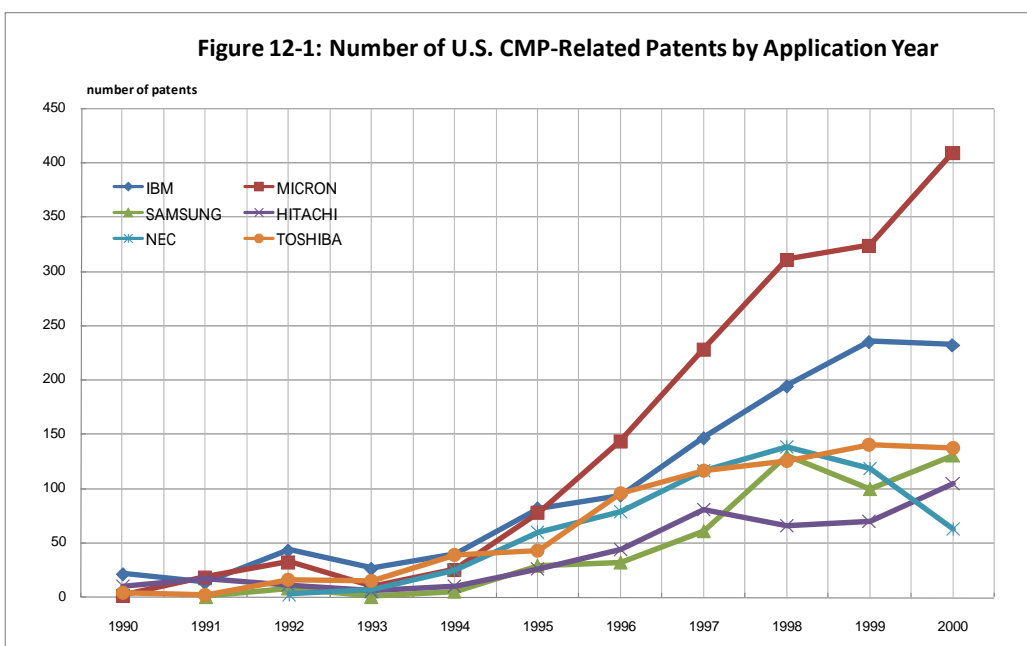


Of course, even if Samsung could have HSG-related process technologies directly from NEC, Samsung still had to effectively integrate and utilize various element technologies with HSG. Indeed, as far as U.S. patents are concerned, both Samsung and Micron registered three-digit numbers of them--119 and 823 patents, respectively--whereas NEC did only 47 patents and Hitachi only 15 patents.⁵³ Such a distinct difference also could be observed in mobilizing human resources for the integration and/or utilization of HSG-related knowledge. Figure 11 shows the transition in “researchers” involved in HSG-related U.S. patents. “Researchers” here are defined as the number of inventors avoiding a double count in each year. Actually, the number of “researchers” in both Samsung and Micron are far larger than that of Japanese competitors. Frankly speaking, with such a huge gap in R&D activities, neither NEC nor Hitachi could have been superior to Micron and Samsung in commercially applying HSG.

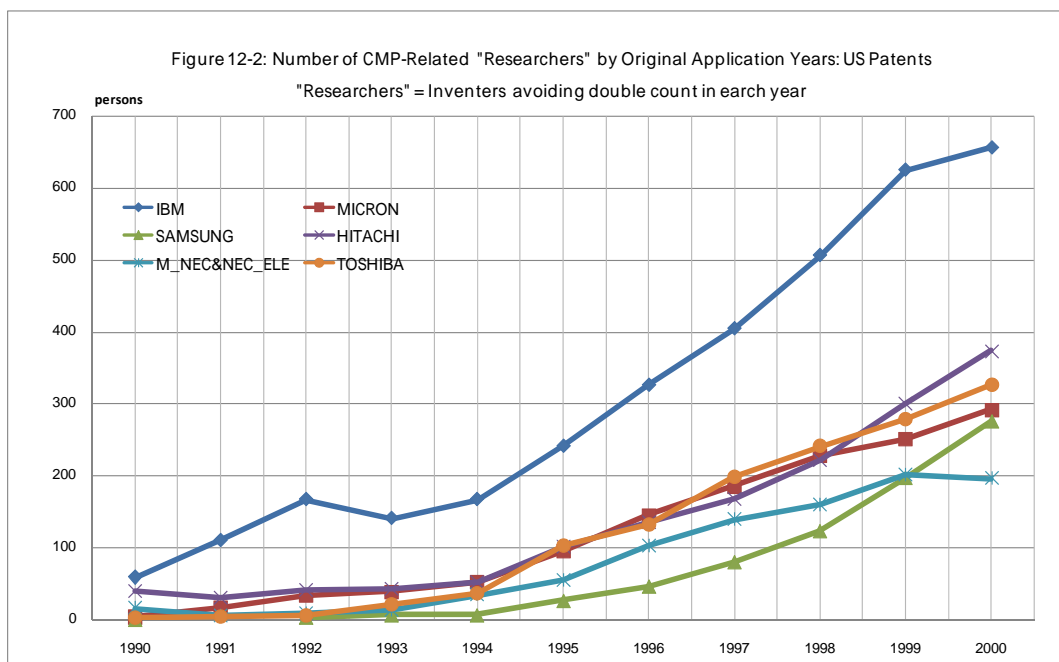
⁵³ In Hitachi, the so-called NIH (Not-Invented-Here) syndrome seemed to have been prevalent.



Lastly, Samsung was very late to commercially apply CMP to both interconnect and transistor layers. For example, Samsung’s 128Mb DRAM in Figure 10 does not use CMP. CMP was first commercially applied to the interconnect layers and ILD (interlayer dielectric) of its 256Mb DRAM in 1998.⁵⁴ Indeed, Figure 12-1 and Figure 12-2 indicate that, except for Micron and IBM, the numbers of CMP-related U.S. patents and “researchers” are even smaller than those of Japanese chipmakers. In this sense, CMP must not be a crucial factor differentiating Samsung from its Japanese counterparts.



⁵⁴ The product is KM44S64230AT-GL.



C. How Could Micron Obtain Mass Production Benefits?

Micron did not pursue pioneers' gains and instead tried to get mass production benefits by quickly shrinking chips. Although Micron invented neither HSG nor CMP, chip shrinking was done by effectively applying both of them to its DRAMs. In particular, Micron's technological advantage was derived from CMP. Such a process is shown in Figure 13, where Micron commercialized 64Mb DRAM in 1997 by applying CMP only to interconnect layers and ILD, and then in 1998 to shallow trench isolation (STI) as well as interconnect layers and ILD. Both chips in this figure display a typical rugged surface of stacked capacitors made by HSG. The effect of STI-CMP on chip shrinking was enormous. Indeed the latter chip (A) became 0.48% smaller in chip-size, 0.55% smaller in cell-size, and 0.57% smaller in transistor gate length than the former (B). If chip-size is 0.48% smaller than before, the number of available chips could be doubled in the case of 200mm wafer. In this sense, the mass production benefits brought about by STI-CMP was quite substantial.

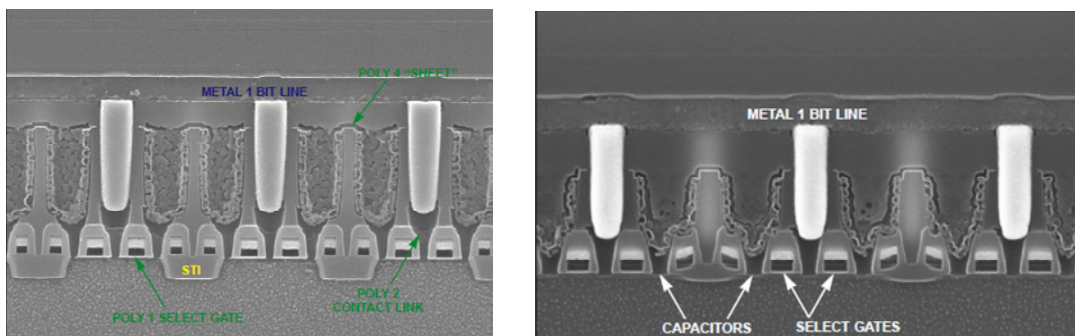
Regarding the reason why even NEC lagged behind Micron in commercially applying HSG, some published data offer an important hint. NEC applied for a Japanese patent on HSG in 1989 and applied for a U.S. patent in 1991. In contrast, Micron applied for a U.S. patent on an HSG-related technology ahead of NEC in January 1990. Moreover, a presentation at the IEDM was made during the same session as NEC in December 1990. In this sense, the patent competition between the two was fierce.⁵⁵

⁵⁵ It is also anecdotally known that Micron and NEC had arranged face-to-face meetings between their topnotch R&D engineers to carry out discussions about HSG (from NEC) and TiN (titanium nitride) CVD technology (from Micron) in the early 1990s. Actually, according to Nikkei Newspaper, both formed the sales alliance in 1992 and the production alliance in 1993. It should be noted here that Micron originally developed to form HSG on the

Figure 13: The Chip-Shrinking Process for Micron's 64Mb DRAM:

(A) 64Mb DRAM: chip-size=59.30 mm², cell-size=0.50μm²

(B) 64Mb DRAM: chip-size=122.70 mm², cell-size=0.80μm²



CMP Applied to	Interconnect Layers and ILD (interlayer dielectric): A	STI (shallow trench isolation): B	Shrin Ratio (B/A)
Chip-Size (mm ²)	59.30	122.70	0.48
Cell-Size (μm ²)	0.500	0.800	0.55
Minimum Gate Length	0.20	0.35	0.57

Courtesy of Chipworks

The central figure in these activities was Dr. Pierre Fazan,⁵⁶ who had joined Micron in 1989. Most of the R&D activities at Micron normally had been done behind the scenes. But those of HSG were exceptional in that Dr. Fazan actively participated in the IEDM to present his academic papers together with his collaborators. Indeed, from 1991 to 1994, he worked with 18 people. The main players among them were two professors from the University of Texas at Austin, together with their nine Ph.D. students. Engineers from RAM Research, Rockwell, and IDT also were included.⁵⁷ This point well exemplifies Micron's broad scope of knowledge utilization beyond the corporate boundary.

As was indicated in Figure 11, as NEC invested in HSG, Micron mobilized a considerable number of engineers or scientists in getting a huge number of HSG-related patents. Related to this fact, the characteristics of those top-ten inventors are very interesting. These topnotch people, three of whom originally worked for IBM, have been involved in 694 patents (84% of the total HSG

(conductive) TiN layer, while most of competitors like NEC did on the (conductive) polysilicon (SiO₂) layer (for details, see U.S. Patent 5612558 by Micron Technology). The utilization of TiN layer, instead of polysilicon one, could guarantee several benefits.

⁵⁶ Dr. Fazan received a Ph.D. in Physics from the Swiss Federal Institute of Technology in Lausanne in 1989 and also is well-known as an inventor of ZRAM (Zero-Capacitor DRAM)

⁵⁷ All of these data are based on the presented papers at IEDM (EDS Archival Collection 1954-2004).

patents). Some of Dr. Fazan’s collaborators noted above also jointly presented academic papers at IEDM with several IBM researchers.

Micron’s broad scope of knowledge utilization beyond corporate boundaries also is exemplified in Figure 12-1, which shows that Micron allocated far more R&D resources to CMP than to HSG. Indeed, the number of CMP-related patents registered by Micron until 2005 exceeded that of IBM by more than 50%, even though the number of “researchers” themselves was much smaller than IBM’s (see also Figure 12-2). Most of the top-ten inventors came from other chipmakers, such as IBM, Philips, Intel, Mostek, or Kodak.⁵⁸

Table 6: Bilaterally Matched Inventors between Micron and Other Makers (CPM-Related U.S. Patents)

Name of Inventors	Patents at Micron	Active Period at Micron	Name of Matched Maker	Patents at the Other Maker	Active Period at the Other Maker	Name of Inventors	Patents at Micron	Active Period at Micron	Name of Matched Maker	Patents at the Other Maker	Active Period at the Other Maker
Jackson; Timothy	4	2000-2003	AMD	2	2001-2003	Zielinski; Eden	2	2000-2002	HP	1	2001-2001
Johnson; William	6	2000-2005	AMD	1	1998-1998	Manzonie; Adam	2	1996-1998	R&H	1	2001-2001
Pan; James	6	1997-2004	AMD	17	2002-2004	Drynan; John	8	2000-2004	NEC	6	1996-1999
Doan; Trung	188	1990-2005	APPLIED	1	2004-2004	Brown; Nathan	9	1999-2005	MOTOROLA	2	2003-2005
Robinson; Karl	93	1995-2004	APPLIED	1	2001-2001	Kim; Sung	6	1993-2000	MOTOROLA	4	1996-1997
Smith; David	1	2001-2001	APPLIED	1	1997-1997	Kirsch; Howard	2	2002-2003	MOTOROLA	2	1992-1993
Thakur; Randhir	66	1998-2002	APPLIED	1	2002-2002	Manzonie; Adam	2	1996-1998	MOTOROLA	1	1997-1997
Schultz; Laurence	7	1990-1999	AT&T	3	1998-1999	Yu; Chris	15	1991-2001	MOTOROLA	10	1993-1995
Yu; Chris	15	1991-2001	CABOT	2	2002-2002	Zhu; Theodore	12	1999-2005	MOTOROLA	3	1997-1999
Lu; Yong	3	2001-2004	CHARTERED	1	2004-2004	Smith; David	1	2001-2001	NOVELLUS	1	2001-2001
Bhattacharyya; Arup	23	2002-2005	IBM	2	1997-1998	Lee; John	39	1995-2003	PROMOS	1	2004-2004
Farrar; Paul	81	1997-2004	IBM	1	1991-1991	Grief; Malcolm	3	1991-1996	SPEEDFAM	4	1999-2003
Givens; John	37	1996-2004	IBM	4	1992-1996	Cho; Chih-Chen	14	2000-2005	TI	2	1999-2001
Jost; Mark	36	1995-2003	IBM	2	1990-1992	Kwok; Siang	2	1999-2000	TI	3	1995-2004
Noble; Wendell	119	1996-2004	IBM	3	1994-1996	Larsen; Jody	3	1995-1999	TI	1	1999-1999
Pan; Pai-Hung	41	1995-2002	IBM	1	1996-1996	Mckee; Jeffrey	1	2002-2002	TI	10	1997-2002
Walker; Michael	67	1992-2003	IBM	1	2002-2002	Richardson; William	2	1999-2000	TI	1	1999-1999
Dennison; Charles	120	1991-2004	INTEL	6	2000-2004	Visokay; Mark	5	2000-2002	TI	16	1998-2005
Johnson; Brian	3	2002-2004	INTEL	1	2002-2002	Wu; Zhiqiang	37	1996-2004	TI	2	2002-2003
Lowrey; Tyler	59	1991-2005	INTEL	7	2000-2003	Zielinski; Eden	2	2000-2002	TI	2	1999-1999
Ryan; Kevin	1	2003-2003	INTEL	1	2002-2002	Li; Li	41	1996-2004	TSMC	1	2004-2004
Sharan; Sujit	32	1994-2004	INTEL	3	2000-2002	Kirsch; Howard	2	2002-2003	VANGUARD	2	1998-1999
Knappenberger; Eric	1	1998-1998	KODAK	1	2001-2001						

Moreover, Micron’s R&D activities across corporate boundaries can be confirmed in Table 6, which was created by bilateral name-matching for U.S. patents between Micron and representative U.S., Asian, or European chip-, tool-, or material-makers. The 3rd and 6th columns show the inventor’s “active” R&D period at Micron or the other maker. The active period at Micron or the other maker is defined as the one in which the corresponding inventor’s patents continuously had applied. By this matching, totally 45 inventors appear to have contributed to the CMP-related

⁵⁸ The data are based on bilateral name-matching between Micron and these chipmakers, as well as internet information.

patents assigned to Micron.⁵⁹ Among them, 21 inventors are estimated to come from or belong to the other makers because their active period at Micron is more recent than the one at the other maker. Moreover, most of them came from IBM (6) or Motorola (5) in the mid 1990s and Texas Instruments (6) in the late 1990s.⁶⁰ These facts properly portray a glimpse into the deep relationships between Micron and IBM or Motorola.

5. Summary

This paper has scrutinized the rise and fall of Japanese chipmakers in the commodity DRAM business during the last three decades. We identified crucial causes and effects related to three kinds of ever-growing complexities: the tardy technology-marketing strategies because of their conventional “linear” (instead of “chain-linked”) R&D models in the face of the fast-moving market complexity, the long persistence of push-systems *cum* in-house MESSs (*vis-à-vis* market-pull systems *cum* Open MESSs) confronting the growing manufacturing system complexity, and the self-reliant diligence in element process technologies despite the growing process complexity beyond corporate boundaries.

The DRAM price per bit gradually decreased by 1/5 during the decade (1985-1995) and dramatically did by 1/250 during the next decade (1995-2005) as the result of a collapse of the commodity DRAM markets in 1996. Such a price freefall brought about drastic structural changes in the semiconductor market as a whole. Especially in commodity DRAM markets, there appeared one noteworthy tendency: that the sizes of commercial DRAMs had quadrupled until 64Mb in a manner like 1Mb→4Mb→16Mb→64Mb, whereas, mainly because of the daunting complexities in process technologies beyond 64Mb DRAM and the dramatic advent of PCs with Windows95/NT, the capacity has come to be duplicated in a manner like 64 Mb→128 Mb→256 Mb→512 Mb. Furthermore, nearly no chips with a size larger than 100 mm² could exist as a mass-produced product any longer.

Most Japanese chipmakers, however, could not effectively cope with this unexpected change. In particular, their misjudgment about the phase change from 64Mb to 128Mb DRAM around 1998 was absolutely fatal, which was intimately related to the stalling speed of synchronization among the research, development, manufacturing and marketing/sales divisions within each corporation. Indeed, most Japanese chipmakers had stuck to conventional linear (sequential) R&D systems, despite their pressing need for chain-linked (concurrent) ones. Consequently, seizing the brief moment when Japanese competitors were pausing for a breath to determine their proper directivity, Samsung jumped into the market in full force to sweep them aside.

⁵⁹ According to Cabot’s various annual reports, “Yu, Chris” who has specialized in CMP, originally came from Motorola, then moved to Micron, and finally to Cabot.

⁶⁰ It is well known that Motorola started to intensively absorb CMP technologies from IBM in 1990 and became a main source of spillovers to various makers (Lim 2000:66).

With the advent of the age of speed-to-market, the importance of cycle-time reduction with a small WIP became one of the vital factors in successfully competing for market advantage. Moreover, in the early 1990s, when commercial production had started on leading-edge 200mm fabs, Moore's law made conventional manufacturing systems "home-grown spaghetti-code monsters" mainly because of the "accelerating-network property" (Mattick and Gagen 2005) between fabrication processes. Around this time, the "Open MES" came about with a look of Toyota or a Lean Manufacturing system (LPS). As has been widely recognized by U.S. (since the late 1980s) and subsequently by European/Korean/Taiwanese chipmakers (since the mid-1990s), the Open MES and LPS (or market pull-system) must have been a lock-and-key concept in the age of speed-to-market.

Most Japanese chipmakers, however, also clung to their own developed MES until the late 1990s and the outdated manufacturing system called a "push-system" until around 2000. The intentional transformation from "autonomic" to "automatic" (manufacturing) systems in face of the enormous extension of interdependence among fabrication processes also brought about a bewildering change in the division of labor among operators/technicians and engineers within many Japanese fabs. As a result, Japanese chipmakers rapidly started to lose their competitiveness even in wafer manufacturing systems. This paper identified, as one of the root causes, Japan's long-established cost management system, the blind use of which was severely criticized by Johnson and Kaplan (1988) as the "Relevance Lost."

Even though DRAM makers could stand out in marketing and manufacturing technologies, it must have been quite difficult to obtain pioneers' gains or mass production benefits (especially through chip-shrinking) without having sufficient science-knowledge integration or utilization capabilities. To understand the key to success, we paid special attention to process technologies called HSG and CMP, which were first applied to 64Mb DRAMs.

According to our analysis based on the microscopic photographs inside each company's 64Mb DRAMs, as NEC invented HSG in the late 1980s, Micron first commercially applied its 64Mb DRAM in 1997 and Samsung did it almost simultaneously with NEC in 1998. Micron's superlative chip-shrink technologies also are confirmed to be effectively accomplished by applying CMP technologies, invented by IBM in the early 1980s, to both interconnect and transistor layers in 1998, one or two years ahead of its Japanese and Korean competitors. We also confirmed that the number of CMP-related patents registered by Micron until 2005 (about 2,800) exceeded that of IBM, the home of CMP, by more than 50%. Both Micron and Samsung had a far greater (three-digit) number of HSG-related patents than NEC or Hitachi. Frankly speaking, with such a huge gap in R&D activities with respect to HSG and/or CMP, even with their basic technological advantages, Japanese (self-sufficient) chipmakers could not have been superior to Micron or Samsung.

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